
On-Wafer Microwave De-Embedding Techniques

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Abstract

Wireless communication technology has kept evolving into higher frequency regime to take advantage of wider data bandwidth and higher speed performance. Successful RF circuit design requires accurate characterization of on-chip devices. This greatly relies on robust de-embedding technique to completely remove surrounding parasitics of pad and interconnects that connect device to measurement probes. Complex interaction of fixture parasitic at high frequency has imposed extreme challenges to de-embedding particularly for lossy complementary metal oxide semiconductor (CMOS) device. A generalized network de-embedding technique that avoids any inaccurate lumped and transmission line assumptions on the pad and interconnects of the test structure is presented. The de-embedding strategy has been validated by producing negligible de-embedding error (<-50 dB) on the insertion loss of the zero-length THRU device. It demonstrates better accuracy than existing de-embedding techniques that are based on lumped pad assumption. For transistor characterization, the de-embedding reference plane could be further shifted to the metal fingers with additional Finger OPEN-SHORT structures. The resulted de-embedded RF parameters of CMOS transistor show good scalability across geometries and negligible frequency dependency of less than 3% for up to 100 GHz. The results reveal the importance of accounting for the parasitic effect of metal fingers for transistor characterization.

Keywords: CMOS, de-embedding, microwave frequencies, scattering parameters, test structure

1. Introduction

Aggressive scaling of complementary metal oxide semiconductor (CMOS) devices over the past decades has led to tremendous increase in speed, making it suitable to be employed in

radio frequency circuits. Current CMOS devices (28 nm) are able to deliver maximum f_t (maximum cut-off frequency) of 340 GHz [1] with superior improvement in noise, power, and gain performance. **Table 1** shows the key comparisons of transistor performance characteristics at various technology nodes.

Technology node (nm)	180	130	90	40	28
Supply voltage (V)	1.8	1.5	1.2	1.1	1.05
Peak cut-off frequency, f_t (GHz)	60	75	140	260	340
Peak transconductance, g_m ($\mu\text{S}/\mu\text{m}$)	562	809	1030	1128	1377

Table 1. Performance-related characteristics of GLOBALFOUNDRIES' NFET (N-type field-effect transistor) at different technology nodes.

However, the growing complexity of radio frequency-integrated circuits requires highly accurate CMOS device model to predict the circuit behavior correctly for successful design. Therefore, accurate and precision RF measurement data are essential to ensure high quality of RF CMOS model developed. Nevertheless, raw measurement data itself does not represent the high-frequency behavior of intrinsic CMOS device as it includes parasitic effects of test structure. Therefore, additional data processing steps, known as de-embedding, are required to remove the impact of test structure parasitic effects from the raw noise measurement data. De-embedding is challenging for RF characterization of short channel device as parasitic effect of interconnects and lossy Si substrate would appear much larger than the device itself. The reason is that interconnects of test structure do not scale proportionally with CMOS device size as minimum distance between probes has to be maintained to avoid collision. Further, the parasitic effects of test structures (i.e. substrate interaction, distributed effect of interconnects, etc.) become more complex at higher measurement frequency and require more sophisticated de-embedding technique. The aim of this chapter is to present an insight of microwave de-embedding theory and knowledge on various techniques to overcome challenges at high frequencies.

Many de-embedding techniques have been reported up to date. They could be broadly classified as lumped circuit model-based technique [2–6] and network model-based technique [7–12]. As the name implies, the aforementioned techniques model the test fixture parasitics as a combination of parallel-series connections of discrete components. Nevertheless, such a de-embedding technique could not be used to address the distributed effect of metal interconnect. In order to overcome the deficiency mentioned, the network model-based de-embedding techniques [7–12] have been proposed. In particular, the technique proposed in Ref. [7] is renowned for its high generality as it models the surrounding fixture parasitic as a single four-port network without any assumptions made on the network topology. However, it requires five test structures and suffers accuracy degradation at very high frequencies due to ideality assumptions made on the intrinsic standards of dummy test structures. Instead, cascade network model-based de-embedding techniques [8–12] offer alternate way to address

the distributed effects of metal interconnects without any precision standards required. Nevertheless, techniques in Refs. [8–11] require lumped assumption on the pad parasitics.

A generalized cascade-based de-embedding technique [12] that addresses the distributed effects of pad and interconnect parasitics will be presented in this chapter. It utilizes unique combination of pad and line de-embedding structures that avoid any lumped assumptions. The description covers parasitic model adopted, de-embedding structures used, and corresponding mathematical de-embedding algorithm in separate subsections. Also, an extension of cascade-based de-embedding technique [13] to further remove the metal finger parasitics of CMOS transistor will be detailed in Section 5. Finally, the validation results of the de-embedding methodology will be presented and supplemented by comparison against existing de-embedding techniques.

2. Test structure

Direct probing on transistor device is impossible due to its minute size. Therefore, test structure is introduced to provide essential electrical interface in between the embedded device and measurement probes through its bond pads and metal interconnections. However, these test fixture components introduce undesirable parasitic effects that lead to error in the device measurements. Particularly, the CMOS test structure is fabricated on silicon substrate that is more lossy than alumina substrate in impedance standard substrate (ISS). One way to reduce the impact of these fixture parasitics is to optimize the design of test structure. **Figure 1(a)** and **(b)** shows the top and cross-sectional view of G-S-G test structure used for characterization of an Negative channel Metal-Oxide Semiconductor (NMOS) device. There are three bond pads with appropriate sizes ($70\ \mu\text{m} \times 60\ \mu\text{m}$) and separation pitches ($50\ \mu\text{m}$) on both side of test fixture for locating the ground and signal probes at each port. Signal interconnects are used to connect gate and drain lead of NMOS devices to bond pads at input and output ports, respectively. As shown in **Figure 1(b)**, it is actually a metal-via stack that consists of three metal layers, Metal 6 to Metal 8 (M6–M8). Sufficient length of interconnects ($>50\ \mu\text{m}$) is required to avoid possible collision and interference between probes. Also, wide interconnects ($10\ \mu\text{m}$) provide low-resistance paths to gate and drain terminals. The test structure is developed based on shielded design [14] where a wide Metal 1 (M1) ground conductor is included to mitigate the substrate coupling effect. It is connected to the ground bars (M1–M8 metal-via stacks) and is tied to silicon substrate through P+ implants. Since the Metal 1 metal shield is large in size, it provides low-resistive ground connections to all ports. Meanwhile, the NMOS device lies inside the fixture gap of Metal 1 shield where it is directly exposed to silicon substrate. **Figure 2** shows the enlarge view of NMOS transistor. The transistor possesses interdigitated layout whereby the source and drain regions are shared for the reduction of parasitic resistance and capacitance. Nevertheless, layout optimization could only partially suppress the fixture parasitic effect, and further de-embedding is required to remove effects of these fixture parasitics from measurements particularly when it gets worsened at high frequencies.

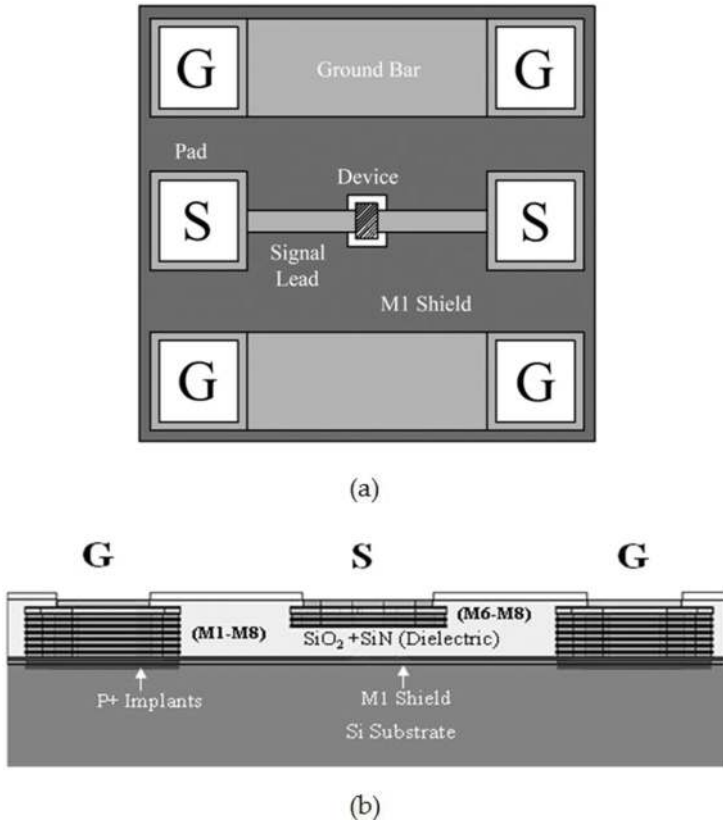


Figure 1. (a) Top schematic and (b) cross-sectional view of transistor test fixture for GHz probing.

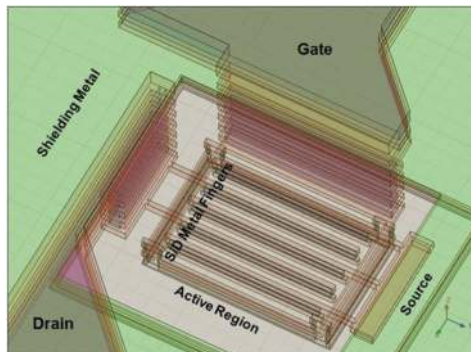


Figure 2. Enlarge view of transistor device embedded in test fixture.

3. Overview of de-embedding techniques

Two popular categories of de-embedding techniques are reviewed theoretically in this section. They are equivalent circuit model-based de-embedding and cascade network model-based de-embedding.

3.1. Equivalent circuit model-based de-embedding

In this method, device (transistor) test fixture is modeled by an equivalent circuit which is basically complex combinations of fixture parasitic components and intrinsic device itself. Network parameters of intrinsic device could be de-embedded from raw S-parameter measurements, provided that the network parameters of fixture parasitic are known. This could be determined through a set of S-parameter measurements on dummy test structures. The number of dummy test structures required typically increase with the complexity of parasitic circuit model. Specifically, open-short de-embedding methodology [2] has been widely adopted for transistor characterization due to its sufficient accurate prediction of fixture parasitic for conventional microwave frequencies of interest at below 30 GHz. As the name implies, it requires an OPEN dummy test structure which consists of only test fixture frame (without intrinsic device) and a SHORT dummy test structure that is associated with short-circuited interconnections for complete characterization of fixture parasitics. The equivalent circuit models of required test structures are shown in **Figure 3**.

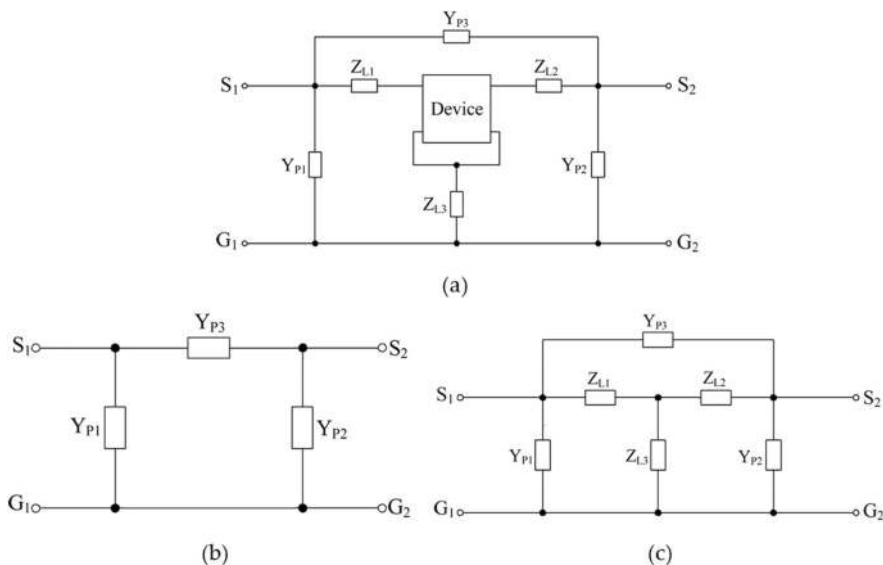


Figure 3. (a) Equivalent circuit model of DUT for open-short de-embedding [6]. (b) π -Circuit model of OPEN dummy test structure. (c) Equivalent circuit model of SHORT dummy test structure for Open-Short de-embedding.

In the device under test (DUT) model (**Figure 3(a)**), admittance component, Y_{p3} , is used to determine the amount of cross talk between port 1 and port 2 due to substrate coupling and fringing capacitances. On the other hand, admittance components, Y_{p1} and Y_{p2} , measure the parasitic capacitances that exist between bond pad and ground for left and right ports. Meanwhile, the metal parasitic components are modeled by a T-network which connected in series with the intrinsic device. Specifically, the series parasitic of metal lines that appear at left and right port is represented by Z_{L1} and Z_{L2} , respectively. Meanwhile, the dangling ground lead parasitic is denoted as Z_{L3} . By employing a two-port network theory for parallel-series network, intrinsic device admittance matrix, Y_{DEV} , could be easily extracted from raw measurements on test structures by Eq. (1).

$$Y_{DEV} = \left[(Y_{DUT} - Y_{OPEN})^{-1} - (Y_{SHORT} - Y_{OPEN})^{-1} \right]^{-1} \quad (1)$$

3.2. Cascade network model-based de-embedding

At much higher frequency where the length of metal interconnects approaches one-tenth of the frequency wavelength, fixture parasitic could no longer be described by lumped circuit model due to worsening of distributed effect. Fortunately, the problem could be overcome with a network model-based de-embedding technique, which is basically the extension of S-parameter probe-tip calibration techniques (SOLT, TRL, LRRM, etc). The cascade configuration model used to describe S-parameter measurement system is now applied on test fixture model instead. The pad and interconnect parasitics of test fixture are now modeled as error adapters connected in cascade with intrinsic device at left and right port. High generality is achieved with this method as interconnect parasitic is characterized by network parameters instead of inaccurate lumped circuit models. Unlike calibration, fixture parasitic is characterized via measurements of de-embedding structures due to unavailability of accurate on-wafer calibration standards. More recently, on-wafer TRL calibration has been reported [15] to directly remove on-wafer parasitics without extra de-embedding steps and known standards needed. However, it is not suitable for modeling since broadband accuracy is unachievable. Also, it is more recommended to be used with expensive gold pads, low substrate loss process, and high layout symmetry for improved accuracy [15].

In conventional cascade-based de-embedding approaches [8–11], probe pads and interconnects of test fixture are characterized by separate networks that are connected in cascade configuration (**Figure 4(a)**). Similarly, THRU structures are used to extract the two-port network parameters or transmission line parameters of interconnects directly. Specifically, the probe pad network is simplified to lumped circuit model which consists of only one parallel admittance element, Y_{PAD} [8, 9], or encompass additional series pad impedance, Z_{PAD} [10, 11]. PAD OPEN structure is commonly used for finding pad to ground admittance, Y_{PAD} , while PAD SHORT structure is used in [10] to determine the series pad impedance, Z_{PAD} . The major drawback of these techniques is that the pad-line discontinuity effect is not accounted, and extraction of series pad impedance is associated with obvious SHORT interconnection parasitic that span from top metal to bottom ground metal. Although no SHORT structure is used in

lumped cascade approach [16], it is unable to account for distributed effects of metallic parasitics. In effort to avoid the deficiencies mentioned, an alternate algorithm has been presented by the authors [11] whereby only THRU structures are used to extract both pad and interconnect parasitics directly. Two set of THRU structures (THRU LL', THRU LH and THRU R'R, THRU RH) are used for determining the network parameters of interconnect at left and right ports, respectively. With each fixture block being characterized using Ref. [11], network parameters of transistor could simply be extracted from raw measurements through chain matrix manipulations as shown in Eq. (2):

$$A_{DEV} = A_{IN}^{-1} A_{DUT} A_{OUT}^{-1} \quad (2)$$

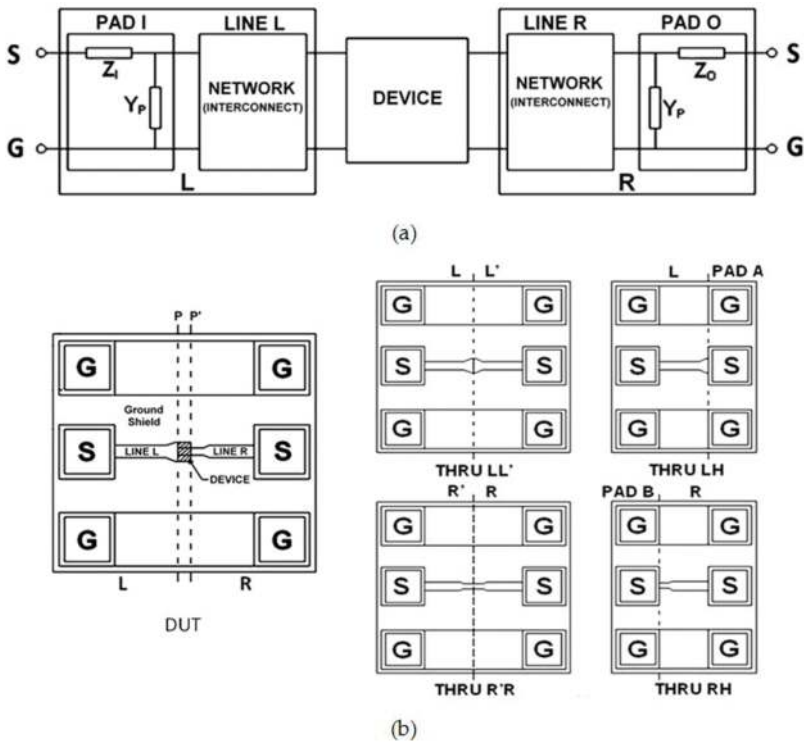


Figure 4. (a) DUT model for author's THRU-based cascade network-based de-embedding approach. (b) Schematic diagram of associated test structures used for author's THRU-based cascade network-based de-embedding technique [11].

For symmetrical DUT structure, the number of THRU structures required for cascade-based de-embedding approach could be reduced further from four to two. Also, the interaction between ports due to leaky substrate and fringing capacitances could be accounted with additional OPEN structure as described in Ref. [17].

4. Generalized cascade-based de-embedding technique

Despite improvement has been made by existing cascade-based de-embedding techniques to address the distributed effects of interconnects, still the pad counterpart is approximated by lumped circuit element. Such issue could potentially be resolved by four-port de-embedding technique in Ref. [7], which avoids any circuit assumption made on the pad and network topology of fixture parasitics. Nevertheless, it requires precision or ideal standards that are unable to be realized on practical CMOS technology. The size of the pad is normally fixed by the dimension of measurement probes and cannot be reduced for optimization of parasitics. As a results, the pad length could become comparable with interconnect length that is usually optimized to be short for parasitic reduction. In effort to overcome the drawback mentioned, a generalized cascade-based de-embedding technique [12] is presented in this section. It utilizes unique combinations of two THRU structures that enable efficient de-embedding of fixture parasitics without any inaccurate lumped pad approximation or requirement of known standards.

4.1. De-embedding concept

Similar to existing cascade de-embedding approaches describe in Section 4, the DUT structure is represented by interconnections of input (L) and output (R) network adapters that appear at both ports of the embedded device (Figure 5(b)). Shielded-based test structure is used here to mitigate the forward coupling effect between two ports [14] as described in Section 2. These fixture network adapters (L, R) include the parasitic contribution of probe pads and metal lines of arbitrary lengths (x_1, x_2). The main advantage of this de-embedding technique is that it does not require any lumped assumption on the pad parasitics since the network parameters of the fixture adapters could be computed directly from measurements on designated de-embedding structures described in the next subsection.

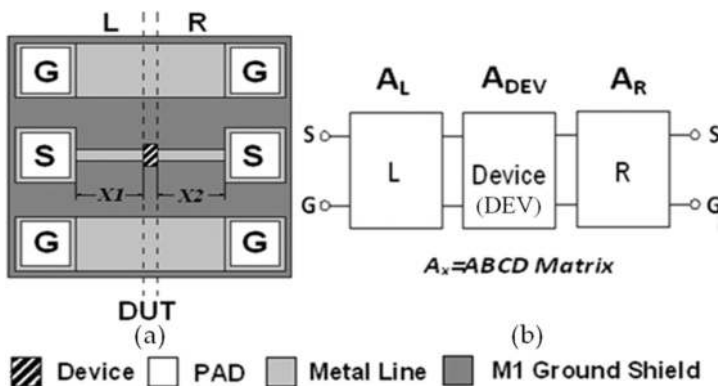


Figure 5. (a) Shielded DUT structure used in device measurement. (b) It is modeled as cascade connections of fixture parasitic networks (L, R) and device [12].

4.2. De-embedding structure

As illustrated in **Figure 6(a)**, two types of THRU de-embedding structures are adopted for extraction of fixture parasitics, namely, THRU LLR and THRU LR structures. The THRU LR structure is simply direct connections of left and right half of test fixture excluding embedded device. Thus, its bond pads and metal line have the same total length as those in DUT structure. Meanwhile, the THRU LLR structure is equivalent to direct connections of left half section of test fixture to the left port of THRU LR structure. Based on the physical layout of the de-embedding structures described, their two-port network models could be determined as illustrated in **Figure 6(b)**. Thus, their cascade matrix (A_{LR} , A_{LLR}) are related to those of fixture parasitic networks (A_L , A_R) by Eq. (3):

$$A_{LR} = A_L A_R \text{ and } A_{LLR} = A_L A_L A_R. \tag{3}$$

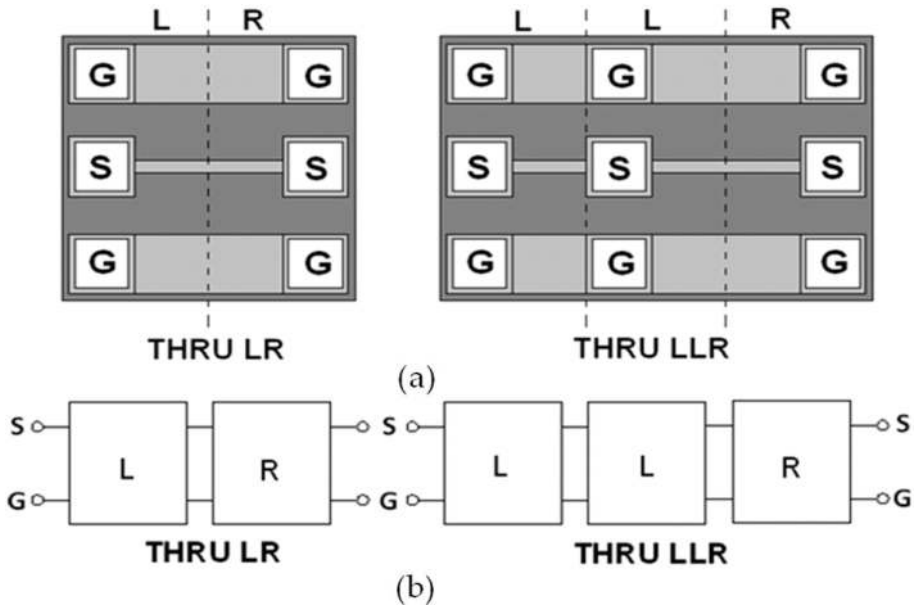


Figure 6. (a) De-embedding structures (THRU LR, THRU LLR) used. (b) They are equivalent to cascade connections of fixture network adapters (L, R) [12].

4.3. De-embedding procedures

The procedure for S-parameter de-embedding is listed as follows:

1. Measure S-parameters of all test structures and convert them into ABCD matrices (A_{DUT} , A_{LR} , and A_{LLR}).

2. Based on the ABCD matrix expression above, determine A_L by $A_{LLR}A_{LR}^{-1}$ and A_R by $A_L^{-1}A_{LR}$ with A_L computed.
3. Finally, de-embed both A_L and A_R from measured ABCD matrix of DUT, A_{DUT} , by Eq. (4) to obtain A_{DEV} :

$$A_{DEV} = A_L^{-1}A_{DUT}A_R^{-1} \quad (4)$$

Further correction of forward coupling effect could be achieved with additional OPEN structure as detailed in Ref. [17]. Overall, the generality of the de-embedding technique is improved as the cascade network parameters determined (A_L , A_R) are valid regardless of their internal circuit configuration. Besides that, the de-embedding methodology is greatly simplified as no determination of pad parasitics or transmission line parameters are required.

4.4. De-embedding validation

In order to validate the de-embedding technique presented above, measurements are carried out on test structures using the E8361 PNA and calibrated to probe tips using LRRM technique [18]. The DUT used for validation has symmetrical layout ($x_1 = x_2$) whereby both halves of test fixture are mirrored copies of each other. For such condition, the ABCD matrices of L and R parasitic networks are related by $A_L = IA_R^{-1}I$ and vice versa $A_R = IA_L^{-1}I$ where $I = \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix}$ is the permutation matrix. Possible extraction errors due to process variations in between the test structures could be minimized by arithmetic averaging of A_L (or A_R) with $IA_R^{-1}I$ (or $IA_L^{-1}I$). Here, the de-embedding validation is performed on 0.13 μm CMOS devices and compared with other techniques [2, 9].

4.4.1. Verification on zero-length THRU

The de-embedding accuracy of interconnect and pad parasitics is verified on THRU device of zero electrical length. Theoretically, it exhibits constant transmission coefficient S_{21} of 1 across frequencies since no parasitics associated with its intrinsic behavior. This could be done by applying de-embedding on the THRU LR structure where interconnects at both ports are connected. The deviations of de-embedded S_{21} from theoretical value are shown in **Figure 7**. Note that the de-embedding error by conventional OPEN-SHORT de-embedding technique [2] is relatively higher than the cascade-based methods in [9] and current work due to inaccurate lumped approximations of fixture parasitic. These results show that the proposed de-embedding method is more accurate than [9] at high frequencies (S_{21} error < 0.01 at 50 GHz) since no lumped pad assumption is made in the fixture model.

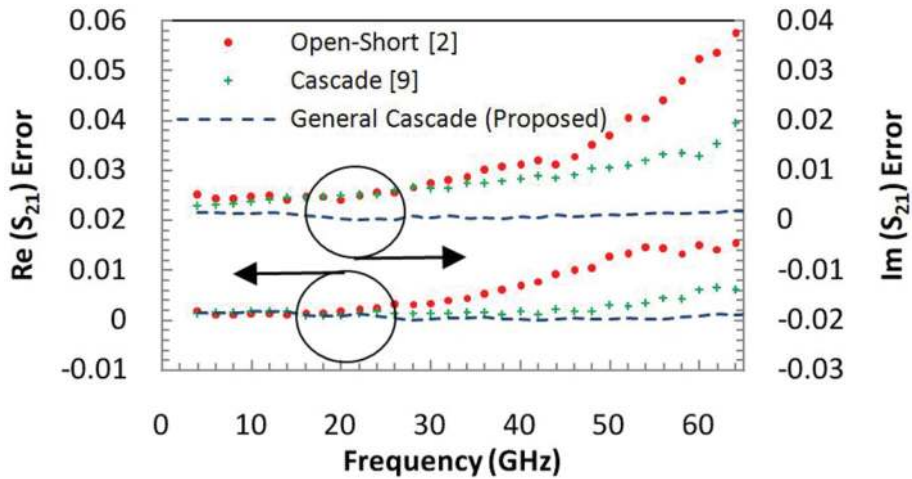


Figure 7. De-embedded S_{21} (real and imaginary) of THRU device versus frequency [12].

4.4.2. Frequency dependencies of transistor parameters

Next, the de-embedding techniques proposed in the current work are validated on frequency dependencies of transistor gate capacitances, C_{gg0} , C_{gd0} , and transconductance, g_m . **Figure 8(a)** shows the de-embedded transistor gate capacitances (width = 32 μm , length = 0.13 μm) at zero DC biases where no quasi static effects occur. It could be calculated from $\text{Im}(Y_{11\text{DEV}})/\omega$ [19]. Under such circumstances, the transistor gate capacitance exhibits constant behavior across frequencies. The de-embedded C_{gg0} by the de-embedding technique in current work reflects physical behavior described since it is nearly independent of frequencies. It varies only by 2.3% for frequency span of 64 GHz when compared to 10% and 5% by Koolen et al. [2] and Cho et al. [9], respectively. Note that the study by Cho et al. [9] shows more physical results than the study by Koolen et al. [2] as the distributed effects of metal lead are taken into consideration. Still, it demonstrates less physical results than proposed de-embedding technique as the distributed effects of pad are ignored. Meanwhile, the transistor gate drain capacitance could be extracted by $(-\text{Im}(Y_{12\text{DEV}})/\omega)$. **Figure 8(a)** demonstrates the de-embedded transistor gate drain capacitances at zero bias. The comparison of de-embedding results shown is consistent with previous on the order of frequency dependency.

The de-embedding validation discussed is further extended to transconductance of transistor in active region ($V_{gs} = V_{ds} = 1.2 \text{ V}$). It could be extracted from real part of Y-parameters, Y_{21} . The comparison results in **Figure 8(b)** show that the de-embedded g_m by Koolen et al. [2] and Cho et al. [9] unphysically enhanced over wide range of frequencies despite worsening impact of non-quasi static effects [19]. Meanwhile, the de-embedded g_m by the proposed de-embedding technique is more physical as it demonstrates attenuation over 5% at 64 GHz.

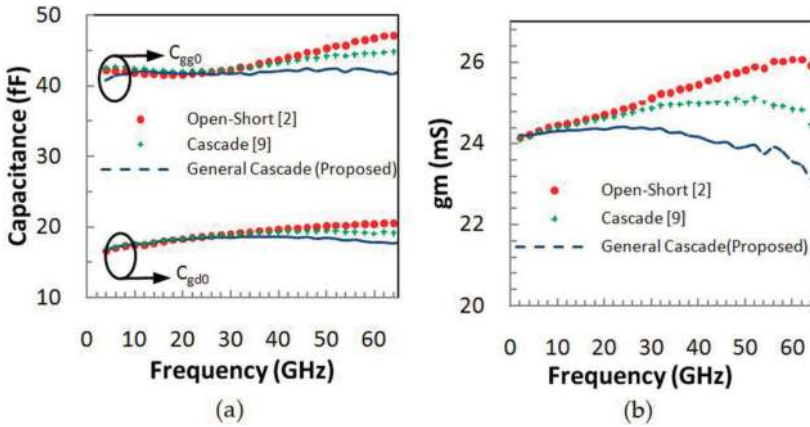


Figure 8. De-embedded parameters of 0.13 μm NMOS transistor versus frequency ((a) C_{gg0} , C_{gd0} , at $V_{gs} = V_{ds} = 0$ V and (b) transconductance, g_m at $V_{gs} = V_{ds} = 1.2$ V) [12].

5. De-embedding metal finger parasitics with hybrid methodology

The de-embedding techniques discussed in previous section focus primarily on removal of pad and interconnect parasitic at top metal level. Nevertheless, it is desirable to establish de-embedding reference plane as close as possible to the device boundary through additional removal of metal fingers parasitic and interconnect via stack. Although several de-embedding techniques [5, 6] have been reported to remove the test fixture parasitics for up to metal fingers, it requires lumped assumptions on interconnects and pad parasitics. Meanwhile, cascade-based de-embedding techniques alone [8–12] are not suitable for removal of metal finger parasitics due to complex inter-couplings between two ports.

In effort to overcome the deficiencies of aforementioned techniques, a hybrid Pad-Line Finger de-embedding technique [13] is presented in this section for mm-wave characterization and modeling of two-port transistor devices. It could simultaneously account for distributed effects of metallic conductors and metal finger parasitics through mix combinations of cascade and lumped series-parallel de-embedding approaches.

5.1. De-embedding concept

Based on the nature of fixture parasitics mentioned, the DUT structure could be described by mix combinations of cascade series-parallel model as shown in **Figure 9**. Similar to de-embedding technique [12] presented in the previous section, metal lines and pads are modeled by generalized cascade network models (PAD, LINE1, 2) to address their transmission line effects. In addition to that, the resistive and coupling characteristics of interdigital fingers are described by series-parallel model (FP, FS).

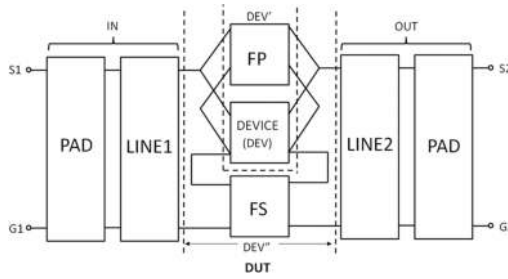


Figure 9. Device under test (DUT) structure modeled as hybrid cascade-series-parallel combinations of two-port device and parasitic networks [13].

5.2. De-embedding structures

Two types of THRU structures (LINE2, PAD-LINE2) are used to extract cascade network parameters of fixture adapters that consist of pad and interconnect parasitics. They consume around 50% less silicon area than those used in the previous section.

As shown in **Figure 10**, the LINE2 structure is equivalent to right half section of DUT structure with pad attached to its left port. On the other hand, the PAD-LINE2 structure differs from LINE2 structure that its left pad is associated with twice of pad length ($2 \times l_{PAD}$). Parasitic extraction for asymmetrical DUT requires additional LINE1 + 2 structure that has total line length of $l_1 + l_2$. It is equivalent to THRU LR structure presented in the previous section. Further extraction of metal finger parasitics is taken care by FINGER OPEN and FINGER SHORT structures. They differ from existing OPEN and SHORT structures that the metal fingers exist in their layouts. Specifically, the FINGER OPEN structure is the same copy of DUT structure but without active region lies underneath the metal fingers. Finally, the FINGER SHORT is similar to FINGER OPEN structure but with source-drain fingers extended and shorted to the gate metals at both ends. Based on the layout configurations, the equivalent network models of the de-embedding structures could be determined as illustrated in **Figure 11**.

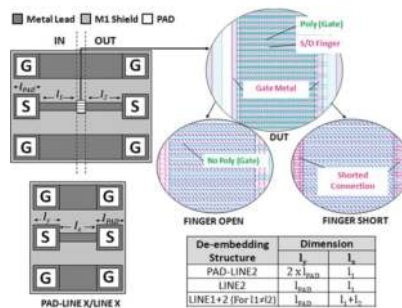


Figure 10. Schematic layout of DUT and de-embedding structures used [13].

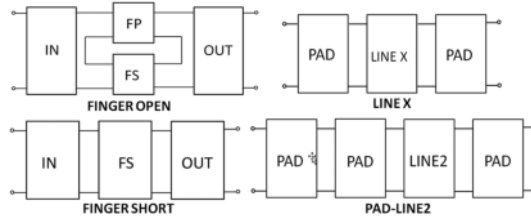


Figure 11. Equivalent parasitic network models of de-embedding structures [13].

5.3. De-embedding procedure

The de-embedding procedure is summarized as follows:

1. Measure S-parameters of all test structures and convert them into cascade ABCD matrices (A_{DUT} , A_{LINE2} , $A_{PAD-LINE2}$, $A_{FINGER OPEN}$, $A_{FINGER SHORT}$, and optional $A_{LINE1+2}$).

2. Compute ABCD matrix of input pad by Eq. (5):

$$A_{PAD} = A_{PAD-LINE2} A_{LINE2}^{-1} \tag{5}$$

3. Compute ABCD matrix of output half fixture by Eq. (6):

$$A_{OUT} = A_{PAD}^{-1} A_{LINE2} \tag{6}$$

4. Compute ABCD matrix of input half fixture by Eq. (7):

$$A_{IN} = I A_{OUT}^{-1} I \text{ or } A_{IN} = A_{LINE1+2} A_{OUT}^{-1} \text{ for the case of } l1 \neq l2 \text{ where, } I = \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix} \tag{7}$$

5. Calculate the resultant ABCD matrix, A_{DEV} after de-embed the cascade parasitic network components using Eq. (8):

$$A_{DEV} = A_{IN}^{-1} A_{DUT} A_{OUT}^{-1} \tag{8}$$

Convert the de-embedded results into Z-matrix, Z_{DEV} .

6. Compute ABCD matrix of series parasitic network by Eq. (9):

$$A_{FS} = A_{IN}^{-1} A_{FINGERSHORT} A_{OUT}^{-1} \tag{9}$$

and convert A_{FS} into equivalent Y-matrix, Y_{FS} .

7. Compute Z-matrix of parallel FP network by $Z_{FP} = Z'_{FP} - Z_{FS}$ where ABCD matrix of Z'_{FP} is computed from $A_{IN}^{-1} A_{FINGEROPEN} A_{OUT}^{-1}$. Convert Z_{FP} into equivalent Y-matrix, Y_{FP} .

8. De-embed series metallic parasitic of routing fingers by Eq. (10):

$$Z_{DEV'} = Z_{DEV''} - Z_{FS} \tag{10}$$

9. Finally, de-embed parallel coupling parasitic of fingers by Eq. (11):

$$Y_{DEV'} = Y_{DEV''} - Y_{FP} \tag{11}$$

5.4. De-embedding results and discussion

In this section, the de-embedding methodology presented is verified and demonstrated on various performance parameters of the 40 nm CMOS transistor. Specifically, the de-embedding results are supplemented by comparisons with [9] to investigate the impact of metal finger parasitic on transistor de-embedding. The experimental results discussed are based on the same measurement setup as previous with exception that the characterization frequency is further extended up to 100 GHz for benchmarking against [2] and previous work [6].

5.4.1. Verification against electromagnetic simulation

The extracted insertion loss of cascade parasitics at input (IN) and output (OUT) port is validated against electromagnetic simulation (EM) by Integrand’s EMX tool. It generates electromagnetic simulations based on boundary element method. As shown in **Figure 12**, the extracted and simulation results agree well with each other. The deviation error of extracted results is within 2% for entire frequency span of 100 GHz.

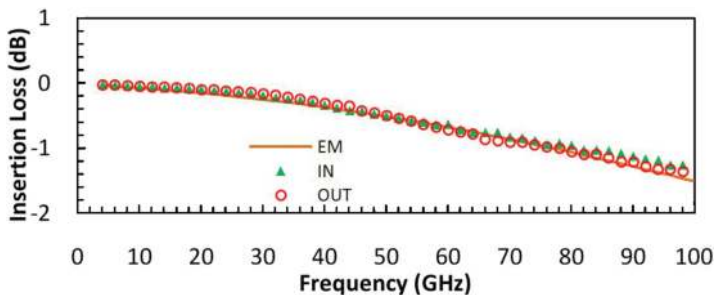


Figure 12. Simulated and extracted insertion loss of input (IN) and output (OUT) network [13].

5.4.2. Scalability of transistor gate capacitance

De-embedding verification on the scalability of transistor gate capacitance provides useful indication on whether the de-embedding technique is correctly applied for up to metal finger. It could be extracted directly from de-embedded Y-parameters ($\text{Im}(Y_{\text{DEV},11})/\omega$) [20] as mentioned in previous section. Interestingly, it becomes frequency independent when the non-quasi static effect of the transistor is negligible. This occurs when the transistor is in cut-off mode since no transcapacitance exists in between its gate and drain terminals [21]. **Figure 13** shows the frequency characteristics of de-embedded gate capacitances across different width geometries of transistors at zero bias and frequency of 8 GHz. They are compared against simulation results by GLOBALFOUNDRIES' 40 nm CMOS model. The results clearly show that the de-embedded transistor gate capacitance by the proposed distributed hybrid de-embedding method is scalable and closely agrees with the simulation results. Meanwhile, the de-embedded results by existing cascade-based de-embedding [9] demonstrate larger gap and less scalability. This shows that exclusion of metal finger parasitics in de-embedding has clear impact even at low frequency.

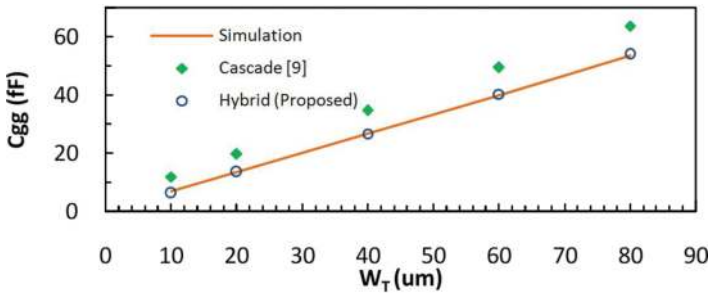


Figure 13. Simulated and de-embedded total gate capacitances of 40 nm NMOS transistor across width geometries at $V_{\text{GS}} = 1.1$ V, $V_{\text{DS}} = 1.1$ V, and 8 GHz [13].

5.4.3. Frequency variability of de-embedded transistor parameters

In this section, the frequency variability of de-embedded transistor parameters is examined for up to 100 GHz. **Figure 14** shows the comparison of extracted transconductance ($\text{Real}(Y_{21})$) by different de-embedding techniques for reference plane established underneath metal fingers. As compared to Refs. [2, 6], the extracted transconductance by the proposed de-embedding technique is almost constant with variation of only 1 ms at 100 GHz. The result is physical as non-quasi static effect of 40 nm transistor is negligible for frequencies below 100 GHz and at strong inversion regime [22]. The frequency variability of de-embedded transistor gate capacitance is further examined for drain bias at 0 V. In such case, the characteristic of CMOS transistor could be described by a passive capacitor. As demonstrated in **Figure 15**, the proposed hybrid de-embedding technique has shown to be more robust than previous work by Loo et al. [6] and Koolen et al. [2] as the maximum variation of de-embedded C_{gg} is within 3% for frequency span of 100 GHz. Similar to previous verification

results, the larger de-embedding error exhibited by Koolen et al. [2] for frequencies beyond 30 GHz indicates that the behavior of test fixture parasitics could no longer be sufficiently described by single stage of parallel-series lumped equivalent circuit. Although greater improvement has been made by Loo et al. [6] with more comprehensive test fixture model, still it suffers larger error than the proposed de-embedding technique due to lumped approximation of metallic conductors. Finally, the frequency dependency of de-embedded maximum current gain bandwidth product ($H_{21} \times \Delta f$) is examined. Theoretically, it is frequency invariant since the maximum current gain of CMOS transistor degrades at constant rate of 20 dB/decade. As illustrated in **Figure 16**, the extracted gain bandwidth product by the proposed hybrid de-embedding technique is more physical since it is almost frequency independent with only 2.1% variation from low frequency value at 100GHz. Comparatively, the de-embedded results by [2, 6] reveal more than 4% error at 100 GHz due to the aforementioned reasons. Note that the transistor gain parameter is more immune to de-embedding error in [2] as it is function of ratio in between transconductance and total gate capacitance.

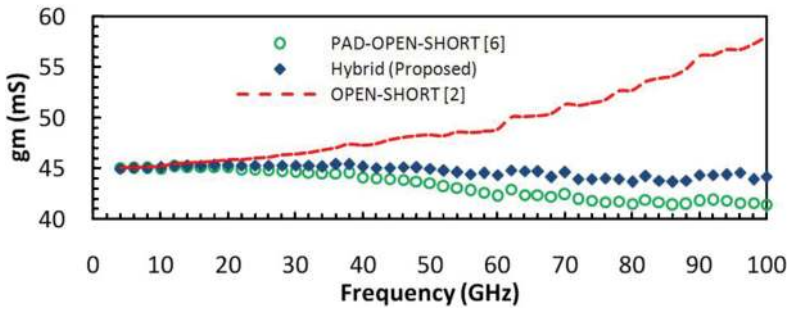


Figure 14. De-embedded transconductance, g_m of 40 nm NMOS transistor ($W_T = 40 \mu m$) at $V_{gs} = 1.1 V$, $V_{ds} = 1.1 V$ [13].

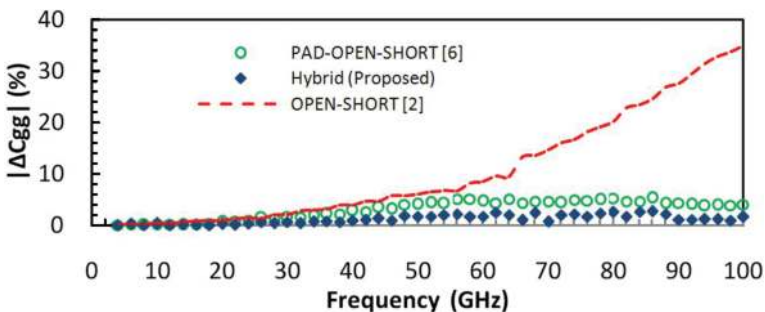


Figure 15. Frequency variability of de-embedded total gate capacitance C_{gg} of 40 nm NMOS transistor ($W_T = 40 \mu m$) at $V_{gs} = 1.1 V$, $V_{ds} = 0 V$ [13].

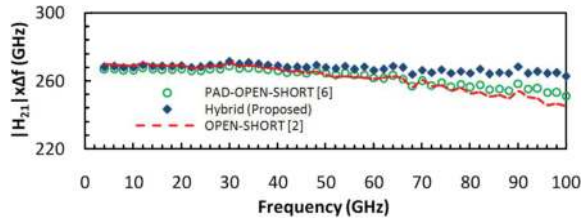


Figure 16. De-embedded maximum current gain bandwidth product, $|H_{21}| \cdot \Delta f$ of 40 nm NMOS transistor ($W_T = 40 \mu\text{m}$) at $V_{ds} = 1.1 \text{ V}$.

6. Conclusion

This chapter presents a generalized network de-embedding technique that avoids any inaccurate lumped and transmission line assumptions on the pad and interconnects of the test structure. The de-embedding strategy has been validated by producing negligible de-embedding error ($< -50 \text{ dB}$) on the insertion loss of the zero-length THRU device. It demonstrates better accuracy than existing de-embedding techniques that are based on lumped pad assumption. For transistor characterization, the de-embedding reference plane could be further shifted to the metal fingers with additional Finger OPEN-SHORT structures. The resulted de-embedded RF parameters of CMOS transistor show good scalability across geometries and negligible frequency dependency of less than 3% for up to 100 GHz. The de-embedding findings suggest that the parasitic effects of metal fingers could not be ignored in modeling of intrinsic transistors. Also, the distributed effect of metallic conductors has to be considered when the line length is comparable to 1/20 of frequency wavelength.

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