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Design and implementation of ultra-wide-band CMOS LC filter LNA

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1. Introduction

Demand for low cost and high data-rate wireless communication systems is increasing. Since the FCC has authorized communication in the 3.1 GHz to 10.6 GHz frequency band, several technologies have been developed to satisfy the communication market. Typically, Orthogonal Frequency Division Multiplexing (OFDM) technique appears to be good candidate for high speed data communication whereas carrier less Impulse Radio (IR-UWB) is a good solution for low cost systems or positioning systems. The allocated frequency bands for UWB are 3.1–10.6 GHz in North America, 6–8.5 GHz in Europe, and 3.4–4.8 GHz, 7.25–10.25 GHz in Japan.
In integrated UWB systems the LNA must provides a high voltage gain on a high impedance output load given by a digitizer or a pulse detector in Impulse Radio UWB architectures, or by a mixer in OFDM architectures. So the LNA is one of the most important analog bloc of the receiver. To achieve low cost the LNA must be fully integrated and must consume low power and low die area. Ideally the LNA must be broadband matched to a 50Ω antenna, and must provide a high voltage gain on a high impedance value capacitive output load. In addition a constant group delay is required in the signal bandwidth to maintain the signal integrity of the pulsed wideband signal.

2. Review of wide band CMOS low noise amplifiers architectures

Architectures allowing large bandwidths are numerous. The main architectures used in CMOS technology in the frequency ranges considered here are:
(i) Distributed Amplifiers, (ii) Feedback Amplifiers, (iii) Common Gate Amplifier, and (iiii) LC Filter LNA.
These architectures can be combined with techniques allowing a bandwidth enhancement as shunt or series peaking, or with techniques allowing the noise figure reduction as the noise cancelation technique.

2.1 Distributed Amplifiers

Among all the broadband amplifier topologies the distributed amplifier architecture is certainly the most powerful in term of bandwidth which can be obtained with a given technology. The principle of the distributed amplifier is to produce two artificial transmission lines coupled by several elementary amplifiers. The input and output capacitor of the elementary amplifiers are all or part of the capacitors constituting the transmission lines (Ginzton et al., 1948). The inductive part of the artificial transmission lines is synthesized by either inductors or by sections of transmission lines. In this topology the amplifier stages are not cascaded, but in parallel. Therefore distributed amplifiers provide lower gains compared with other architectures, but theirs main advantage is the ability to achieve very large bandwidths. In addition, these amplifiers provide a constant group delay over the entire bandwidth and they can be used in the context of pulse-type signals of very large bandwidth. The main disadvantages are the silicon area used to synthesize artificial transmission lines, and a heavy DC power consumption resulting from the numerous stages commonly required to obtain an high gain value.

Zhang (Zhang & Kinget, 2006) has used a distributed amplifier architecture to design a UWB LNA in a 0.18µm CMOS technology. The strength of this design is the power consumption which is below 10 mW. This low DC power consumption for a distributed amplifier has been obtained by using a low number of stages and also by biasing the MOS transistors in a weak inversion mode. But, as expected, the power gain is low (8dB) and also the silicon area is high (1.16 mm^2) because of the great number of spiral inductors (8).

Heydari (Heydari, 2007) has also used a distributed amplifier architecture in a 0.18µm CMOS technology. The originality of this design is to use bandwidth enhancing inductors. So the full FCC bandwidth is obtained with a good noise figure but with high power consumption (21mW). However the gain is low (8dB) and the number of inductors very high (11 spiral inductors).

2.2 Feedback Amplifiers

Another widely used broadband topology is the feedback architecture. The principle is to exchange gain with bandwidth. A shown in Fig. 1, a simple way to implement a feedback amplifier is to insert a resistor between the input and the output of a voltage amplifier implemented here by a cascode stage.

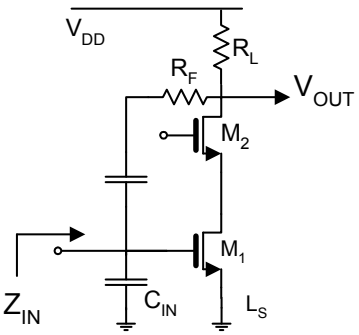

Fig. 1. Resistive feedback amplifier basic topology

C_{IN} is the total amount of input capacitance of the cascode amplifier stage. The voltage amplification in the low frequency range is given by (1) and the input impedance Z_{IN} by (2) and (3). In the low frequency range Z_{IN} is roughly equal to $1/g_{m1}$ if the transconductance value is high.

$$A_v = -\frac{g_{m1}.R_F - 1}{1 + R_F / R_L} \tag{1}$$

$$Z_{IN} = R_{IN} // C_{IN} \tag{2}$$

$$R_{IN} = \frac{R_L + R_F}{1 + g_{m1}.R_L} \tag{3}$$

To obtain a power matching in the low frequency range R_{IN} must be equal to the antenna impedance which has generally a standard value of R_0=50Ω. Consequently the 3 dB cut-off frequency directly depends on the input capacitor C_{IN} by (4).

$$f_C = \frac{1}{\pi.R_0.C_{IN}} \tag{4}$$

Therefore the bandwidth is limited by the input capacitor C_{IN} which is mainly the C_{GS} of the input MOSFET. If a 50Ω input matching is required in a given bandwidth f_{max} the size of the input MOSFET is limited and that leads to poor amplification and noise performances in CMOS technologies. A larger MOS size can be used by adding an inductor at the input but at the expense of a higher silicon area.

Such resistive feedback topology has been used by Kim in a 0.18µm CMOS technology (Kim et al., 2005). This amplifier uses an active load, and a bandwidth enhancing inductor to obtain more gain. It also uses an inductive series peaking in the first and second stage load. The measured power gain is 13.5 dB with 25mW DC power consumption. The noise figure is lower than 7dB in the 2-9 GHz frequency range and this LNA uses 3 inductors.

Reiha has used a feedback topology in a 0.13µm technology (Reiha et Long, 2007). However in this design the feedback is implemented by means of on chip inductive transformers. The full 3.1-10.6 GHz FCC bandwidth is obtained with a high gain (15dB), a low noise figure (less than 2.1dB) and furthermore with a DC power consumption less than 10 mW. Nevertheless this LNA shows a non linear phase response leading to a non constant group delay in the bandwidth which can lead to a distortion of the received pulse. But the main drawback of this design is the use of on chip transformers which are note always available in CMOS technologies.

2.3 Common gate Amplifiers

The common gate topology is also a simple way to obtain a wide band amplifier. Indeed a 50 Ω input matching can be obtained just by setting the g_m of the input MOSFET at the value of 20 mS. The LNA bandwidth is limited by the input capacitor which is mainly the C_{GS} of

the input MOSFET. So, like in the case of the resistive feedback topology, the size of the input MOSFET is limited by the bandwidth. That leads in CMOS technologies to a poor gain performance. So bandwidth extension techniques must generally be used at the expense of silicon area. Another drawback of this topology is that simultaneous power and noise matching is not possible. So if this LNA architecture is used without additional techniques such as noise cancellation the noise figure is very high.
Chen has used the Common Gate topology to design an UWB LNA in a 0.18μm CMOS technology (Chen & Huang, 2007). The first stage is a common gate stage with a bandwidth enhancing inductor, and the second stage is a cascode stage with an inductive series peaking. As expected the noise figure is high especially in the high frequency range (6.5dB@10GHz). The main advantage of this LNA is the low number of spiral inductors.

Liao has used the noise cancellation technique to lower the noise figure of the common gate topology (Liao & Liu., 2007). The noise cancellation principle is to add a second path between the input and the output. For the signal these two paths are in phase, but the noise current generates to opposite voltages at the input of these two paths and so the noise is cancelled at the output. This way this LNA shows a noise figure performance (5dB@10GHz) better than the previous LNA despite they are both designed in the same technology. However the drawbacks of noise cancellation technique are an increase of the DC power consumption and of the silicon area. Indeed this LNA consumes 20mW and uses 5 spiral inductors.

2.4 LC filters Amplifiers

In LC filter amplifier architecture the input matching cell is designed with inductors and capacitors like in a standard band-pass filter. So the LNA frequency response is accurately defined with a given center frequency, a given fractional bandwidth and a given ripple. The input MOSFET is embedded in the LC filter architecture (see Fig. 2). The input MOSFET is sized so its input capacitor matches the series capacitor of a ladder LC filter. The filter resistive termination is synthesized by the inductive degeneration of the input MOS M_1 provided by L_S. The strength of this architecture is to provide a well controlled band-pass response. This band-pass response reduces the noise equivalent bandwidth and so the noise output voltage. The main drawback is to need necessarily inductors and so low silicon area cannot be addressed with this architecture.

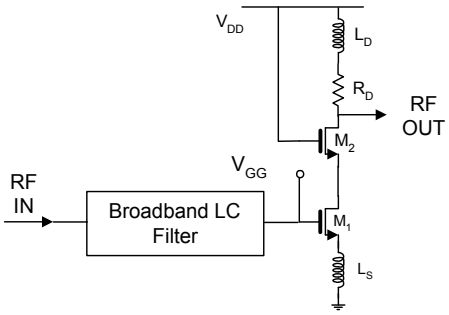

Fig. 2. LC filter amplifier topology

Bevilacqua has implemented a third order Tchehebytcheff band-pass input matching cell in a 0.18μm CMOS technology (Bevilacqua & Nikenejad, 2004). This LNA uses five spiral inductors and consequently consumes a large silicon area. The power consumption is low (9 mW) but the noise figure is high especially in the high frequency range (8dB@9.5GHz). The low noise figure performance is due to the large number of inductors between the input and the first amplification stage. The strength of this design is its high selectivity in comparison to previous architectures.
Battista has implemented a LC filter LNA in a 0.13 μm CMOS technology with a second order Tchehebytcheff band-pass input matching cell (Battista et al., 2008, a). Comparatively to a third order response the number of spiral inductors is reduced in the input matching cell and consequently there are less lossy inductors between the input and the gate of the input MOSFET. So a better noise performance is obtained especially in the high frequency range (4.8dB@10GHz).
Standard LC ladder filter input matching cell cannot address small fractional bandwidth such as 6-8.5 GHz ECC frequency band. These small fractional bandwidths can be addressed by using an input matching cell architecture using passive admittance inverters (Gaubert et al., 2005).

In the following sections we present a design method for these LC filter amplifiers based on our research works in this area published in (Gaubert et al., 2005), (Battista et al., 2008,a), (Battista et al., 2008,b) and (Battista et al., 2010).

3. LC filter input matching cell design

Two different cases have to be considered depending on the fractional bandwidth value of the input filter. The fractional bandwidth is defined by the absolute bandwidth divided by the center frequency.

3.1 Broadband input matching cell for small fractional bandwidths

If the full 3.1-10.6 GHz FCC UWB frequency band or a large bandwidth is used, then the fractional bandwidth b of the LC ladder input matching cell is around unity. In this case the design method proposed in (Bevilacqua & Nikenejad, 2004) leads to inductor values which can be integrated in standard CMOS technologies. On the other hand when b is smaller than about 50%, the inductor values of input matching cell are much dispersed and the integrated inductors have very low self-frequency resonance (SFR) values or low quality factors Q. (Battista et al., 2008,b). For example the ECC 6-8.5 GHz frequency band allows fractional bandwidth b lower than 35%. Such fractional bandwidths lead to large inductor values with self frequency resonance (SFR) lower than the operating LNA frequencies in traditional LC filter LNA architecture. By using admittance inverters, broadband LC filter input matching cell for small fractional bandwidths can be implemented in standard CMOS technologies (Gaubert et al., 2005).
Such input matching cells are obtained from the band-pass filter using admittance inverters shown in Fig. 3.a. which is equivalent to the classical LC ladder filter shown in Fig. 3.b. This filter can be implemented in CMOS technologies with the architecture shown in Fig. 3.c. The corresponding LNA input matching cell is given in Fig. 3.d. In Fig 3.a, 3.b, and 3.c the element values are normalized by the center frequency of the LNA bandwidth f_0 and by R_0 =

50Ω. In the LNA input matching cell given in Fig. 3.d., the terminating resistance of the input filter is synthesized by the inductive source degeneration of the FET M_1. This architecture allows the choice of arbitrarily values for the input matching cell inductors L_{P1} and L_{P2}. This way, practical inductor values leading to high SFR value and high Q factor can be chosen according to the LNA operating bandwidth. Once the values of inductors L_{P1} and L_{P2} are fixed, relations (5)-(13) give the input matching cell element values for a given power consumption and a given value of the degeneration inductance L_S.

$$z_{IN} = \frac{Z_{IN}}{R_0} = \frac{g_{m1} L_S}{R_0 C_{GS1}} + \frac{j\omega L_S}{R_0} + \frac{1}{j\omega R_0 C_{GS1}} = r_{IN} + j\, x_{IN} \tag{5}$$

$$J_1 = \sqrt{\frac{b}{g_1 \lambda_{P1}}} \tag{6}$$

$$J_2 = \frac{b}{\sqrt{g_1 g_2 \lambda_{P1} \lambda_{P2}}} \tag{7}$$

$$J_3 = \sqrt{\frac{b}{g_2 g_3 r_{IN} \lambda_{P2}}} \tag{8}$$

$$\gamma_{J1} = J_1 \left(1 + J_1^2\right) \tag{9}$$

$$\gamma_{J2} = J_2 \tag{10}$$

$$\gamma_{GS1} = J_3 \left(1 + J_3^2 r_{IN}^2\right) \tag{11}$$

$$\gamma_{P1} = \frac{1}{\lambda_{P1}} - J_1 - J_2 \tag{12}$$

$$\gamma_{P2} = \frac{1}{\lambda_{P2}} - J_2 - J_3 \tag{13}$$

In these expressions $b=(f_{P2}-f_{P1})/f_0$ is the fractional bandwidth, f_{P1} and f_{P2} are respectively the lower and higher cut-off frequencies and f_0 the center frequency of the input filter. g_1, g_2, g_3 are the normalized values of the low-pass equivalent filter, and J_1, J_2, J_3 are the normalized values of the admittance inverters (Zverev, 1967). The values of J_1 and J_3 must be low in comparison to unity in order to match an antenna resistor R_{ANT} of 50Ω.

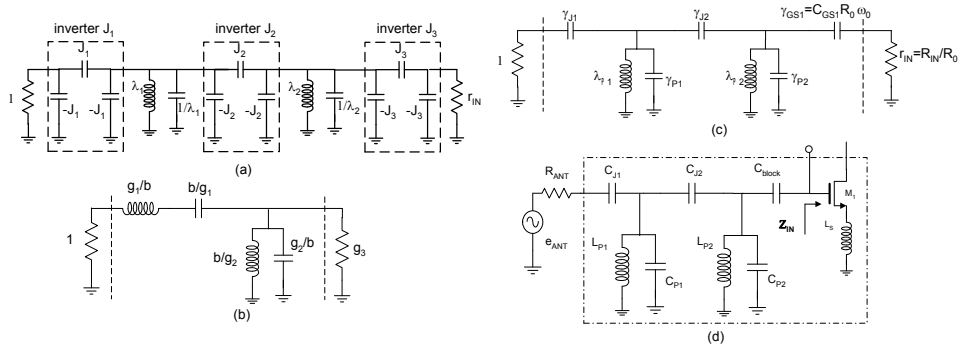

Fig. 3. Single ended broadband input matching cell for small fractional bandwidths. (a) Input matching cell architecture showing the admittance inverters. (b) Equivalent LC ladder filter (c) Input matching cell equivalent circuit. (d) LNA broadband input matching cell architecture.

3.2 Broadband input matching cell for large fractional bandwidths

In the case of large fractional bandwidths such as the full 3.1-10.6 GHz FCC UWB frequency band, the traditional LC filter architecture can be employed (Bevilacqua & Nikenejad, 2004). However a second order input matching cell allows lower number of inductors and consequently less input matching cell losses. The use of a two section LC ladder filter topology with a Tchebycheff second order response allows a noise figure reduction (Battista et al., 2008,a). The corresponding filter topology is shown in Fig. 4.a and the input matching cell of the LNA as shown in Fig. 4.b. In this implementation the series capacitor b/g_2 is synthesized by the MOSFET capacitance C_{GS}, and the series inductor g_2/b is synthesized by L_{S2} in series with L_S.

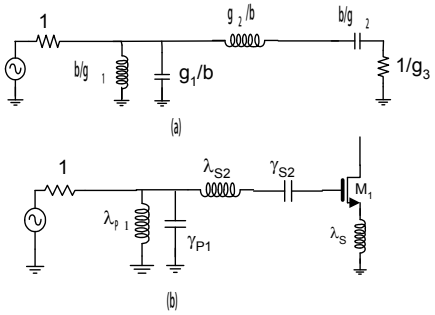

Fig. 4. Input matching cell for large fractional bandwidths. (a) Second order LC ladder filter. (b) Single ended input matching cell implementation.

The element values of the normalized input matching cell are given by relations (14)-(18) where g_i are the normalized values of the second order Tchebycheff Low-Pass ladder filter and b the fractional bandwidth.

$$\gamma_{P1} = \frac{g_1}{b} \tag{14}$$

$$\lambda_{P1} = \frac{b}{g_1} \tag{15}$$

$$\gamma_{GS} = \frac{b}{g_2} \tag{16}$$

$$\lambda_{S2} + \lambda_S = \frac{g_2}{b} \tag{17}$$

$$r_{IN} = \frac{1}{g_3} \tag{18}$$

The overall series inductor value $L_{S2} + L_S$ is reduced by using an even Tchebycheff response. Indeed the normalized value of the corresponding inductor g_2/b is low in such response type. Consequently L_{S2} and L_S are low enough to have good features even in the high range of the UWB frequency band. Comparatively, the use of a third-order response would lead to a series resonator with a normalized inductor value of g_1/b much higher.

4. LC filter LNA architecture analysis

4.1 LNA architecture modeling

The LNA architecture is given in Fig. 5.a. This architecture can be analyzed in the following way (Battista et al., 2008,b).

In the bandwidth the LNA input is power matched to the antenna. Consequently the resistive termination R_{IN} of the input matching cell, provided by the MOSFET M_1 by means of inductive source degeneration, receives an input power equal to the available power P_{AV} at the antenna output given by (19) where e_{ANT} is the open voltage at the antenna and R_{ANT} its radiation resistance.

$$P_{AV} = R_{IN} i_1^2 = \frac{e_{ANT}^2}{4 R_{ANT}} \tag{19}$$

So, in the input filter bandwidth, the magnitude of the current i_1 flowing into the gate of M_1 is given by:

$$i_1 = \frac{e_{ANT}}{\sqrt{4 R_{IN} R_{ANT}}} \tag{20}$$

The equivalent circuits of the first and the second stage are given respectively in Fig. 5.b. and Fig. 5.c. M_2 is loaded by the parallel resonator L_3, C_3, R_3, where C_3 is the overall capacitor at M_2 drain which is given by:

$$c_3 \cong c_{GD2} + c_{DB2} + c_{IN2} \quad (21)$$

where C_{IN2} is the second stage input capacitance. Assuming the effect of C_{GD1}, C_{DB1} and C_{GS2} negligible in the cascode configuration, and neglecting the real part of the input impedance of the second stage, we get:

$$\frac{v_{OUT1}}{\left(e_{ANT}/2\right)} = \frac{L_3}{L_S}\sqrt{\frac{R_{IN}}{R_{ANT}}}\frac{1}{1+\frac{j\omega}{Q_3\omega_{03}}-\left(\frac{\omega}{\omega_{03}}\right)^2} = \frac{A_{V1}}{1+\frac{j\omega}{Q_3\omega_{03}}-\left(\frac{\omega}{\omega_{03}}\right)^2} \quad (22)$$

With

$$Q_3 = \frac{R_3}{L_3\omega_{03}} \qquad \omega_{03} = \frac{1}{\sqrt{L_3C_3}} \quad (23)$$

It should be pointed that (22) is valid only in the LNA bandwidth where the LNA input is power matched to the antenna by the input matching cell. Outside the LNA bandwidth, the input matching cell provides a band-pass response which modifies the output voltage v_{out1}.

The second stage voltage gain A_{V2} can be approximated by (24), where $1/r_{DS3}$ and $1/r_{DS4}$ are the output conductance of M_3 and M_4. R_L and C_L are set by the input impedance of the following stage (see Fig. 5.a).

$$\frac{V_{Out2}}{V_{Out1}} \cong \frac{-g_{m3}r_{EQ}}{1+j\omega/\omega_{C2}} = \frac{A_{V2}}{1+j\omega/\omega_{C2}} \quad (24)$$

where

$$r_{EQ} = r_{DS3} \;//\; r_{DS4} \;//\; R_L \quad (25)$$

$$c_{EQ} = \left(c_{DB3} + c_{GD3} + c_{DB4} + c_{GD4} + c_L\right) \quad (26)$$

$$\omega_{C2} = \frac{1}{r_{EQ}c_{EQ}} = 2\pi f_{C2} \quad (27)$$

Finally the whole LNA voltage amplification in the bandwidth is given by:

$$\frac{v_{OUT2}}{\left(e_{ANT}/2\right)} = \frac{A_{V1}}{1+\frac{j\omega}{Q_3\omega_{03}}-\left(\frac{\omega}{\omega_{03}}\right)^2}\frac{A_{V2}}{1+\frac{j\omega}{\omega_{C2}}} \tag{28}$$

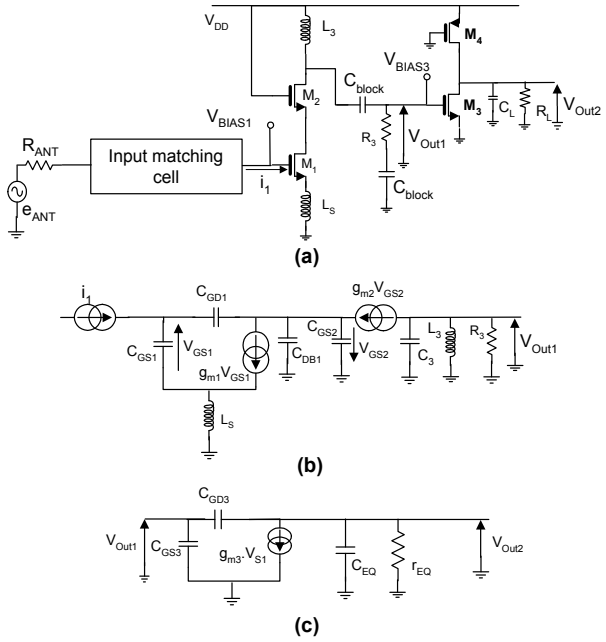

Fig. 5. LNA architecture. (a) LNA architecture. (b) First stage equivalent circuit. (c) Second stage equivalent circuit.

4.2 Noise figure optimization

The goal is to minimize the noise figure at power matching for a given current consumption I_{01} of the LNA first stage.

It is shown in (Nguyen et al., 2004) that the optimum noise impedance Z_{OPT} of the inductively degenerated common source topology is given by:

$$Z_{OPT} = \frac{A}{\omega C_{GS1}} - \frac{B}{j\omega C_{GS1}} - jL_S\omega \tag{29}$$

where A and B are two parameters that only depend on the MOS noise parameters α, δ, γ, c. From (5) and (29) we get:

$$Z_{OPT} - Z_{IN}^{*} = \frac{A}{\omega C_{GS1}} - R_{IN} + \frac{(1-B)}{j\omega C_{GS1}} \tag{30}$$

In order to minimize the noise figure at power matching we can cancel the real part of (30) at a given frequency f by setting M_1 width to fulfil:

$$\gamma_{GS1}\,\Omega = \frac{A}{r_{IN}} \tag{31}$$

In (31) Ω is the normalized frequency f/f_0. It is important to notice that the imaginary part of (30) cannot be cancelled because B is not a design parameter. Indeed B only depends on the used process. From (31) and (5), we obtain the optimal source inductor value:

$$L_{SOPT}\left(\omega\right) = \frac{A}{g_{m1}\omega} \tag{32}$$

For band-pass LNAs the optimal L_S value must be chosen with (32) at the center frequency of the bandwidth f_0. So the discrepancy is less than (b/2)% in the whole LNA bandwidth.

In the case of small fractional bandwidths, an optimal M_1 size can be found to satisfy both (31) for noise minimization and the input matching cell relations (5)-(13). (11) can be approximated by (33) because J_3 must be chosen in order to be low in comparison to unity in the input matching cell design as mentioned above.

$$\gamma_{GS1} \approx J_3 \tag{33}$$

Reporting (33) and (31) in (8) gives (34). (34) gives the optimal MOSFET width as a function of the input filter characteristics (g_1, g_2, g_3, b) and the inductor normalized value λ_{P2}.

$$\gamma_{GS1} = \frac{b\,\Omega}{g_2 g_3 \lambda_{P2} A} \tag{34}$$

In the case of large fractional bandwidths, the size of the MOSFET M_1 is set by (16). From (16), and (31), with (18) we get (35):

$$b = \frac{A g_2 g_3}{\Omega} \tag{35}$$

(35) shows that the noise minimization cannot be achieved for arbitrarily values of the fractional bandwidth b. This issue can be addressed by using the DC blocking capacitor C_{S2} in Fig. 4.b as a design parameter allowing an increase of the M_1 size. This way (16) becomes:

$$\frac{\gamma_{S2}\cdot\gamma_{GS}}{\gamma_{S2}+\gamma_{GS}} = \frac{b}{g_2} \tag{36}$$

and both the noise minimization and the power matching can be achieved by taking a M_1 width leading to (37):

$$\gamma_{GS} = \frac{A.g_3}{\Omega} \tag{37}$$

Provided (38) is satisfied.

$$\gamma_{GS} = \frac{A.g_3}{\Omega} \geq \frac{b}{g_2} \tag{38}$$

If (38) is not satisfied another way is to use a parallel capacitor between the gate and the source terminals of M_1 in order to decrease the value of C_{GS} while satisfying (16).

4.3 Voltage gain maximization

(28) shows that the voltage amplification in the LNA bandwidth results from the product of a second order low pass response by a first order low pass response given by the second stage. A high r_{EQ} value may be used in order to maximize the second stage gain A_{V2}. However a high r_{EQ} value leads to a second stage cut-off frequency lower than the lower cut-off frequencies of the LNA. To overcome this problem, the drop with the frequency of the second stage voltage gain in the LNA bandwidth is compensated by setting the quality factor Q_3 of the second order response greater than $1/\sqrt{2}$.
To maximize A_{V1}, (22) shows that the value of L_3 must be maximum. However the frequency resonance f_{03} of the parallel resonator must be higher than the highest cut-off frequency of the LNA. So, in order to maximize L_3, C_3 must be minimized. In this way we size M_3 much smaller than M_2. In addition M_2 is set to the minimal value which allows the driving of the DC current of the first stage in order to minimize C_{GD2} and C_{DB2}.
To maximize further A_{V1}, (22) shows that L_S must be minimized. However the value of L_S must satisfy the input matching cell relations.

In the case of small fractional bandwidths the input matching cell relations are given by (5)-(13). Taking into account (33), L_S and g_m values are thus linked by (5) and (9) and must satisfy (39):

$$g_m L_S = \frac{b}{\gamma_{GS} g_2 g_3 \omega_0 \lambda_{P2}} \tag{39}$$

So, in this topology, the voltage gain can be increased for the same current consumption by decreasing L_S and by increasing C_{GS} or L_{P2} in order to maintain (39). Another way to increase the voltage gain by decreasing L_S is to maintain the $g_m L_S$ product at a constant value by increasing the current consumption.

In the case of large fractional bandwidths the input matching cell relations are given by (1) and (14)-(18). (1), (16), (18) give (40):

$$g_m L_S = \frac{b}{g_2 g_3 \omega_0} \tag{40}$$

Additionally the size of M_1 is set by (16). Consequently the only way to increase the voltage gain is to decrease L_S while maintaining the $g_m L_S$ product to a constant value by increasing the current consumption.

5. Differential ended architecture

5.1 Differential ended Input matching cell for small fractional bandwidths

The differential ended input matching cell is deduced from the single ended architecture shown in Fig. 3.a (Battista et al., 2010). In this topology the equivalent differential ended cell shown in Fig. 6.a has the same number of inductors than the single ended cell. In order to achieve higher gain, the differential ended input filter implemented in the LNA could be terminated by two cascode common source amplifier with inductive degeneration as shown in Fig 6.c. The element values of the differential ended input matching cell are given by the relations 5-13 like in the single ended matching cell case.

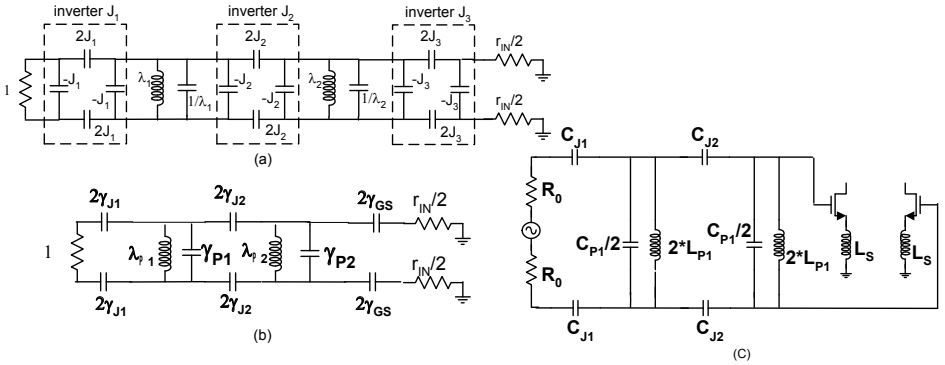

Fig. 6. Differential ended matching cell. (a) Normalized band-pass filter with admittance inverters. (b) Normalized input matching cell. (c) Input matching cell implementation.

5.2 Differential ended Input matching cell for large fractional bandwidths

A differential ended input matching cell implementation, shown in Fig. 7, has been proposed in (Bevilacqua et al., 2006). In order to enhance the amplification performance in the UWB frequency range, two arms, build with common source with inductive degeneration, are preferred to differential transistor pair architecture. Element values of the differential ended input matching cell are deduced from the single ended input matching cell case shown in Fig. 4.b, and can be computed with relations (14) –(18).

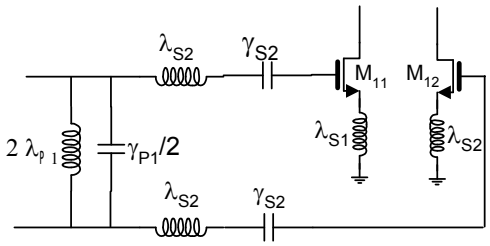

Fig. 7. Input matching cell for large fractional bandwidths. (a) Second order LC ladder filter. (b) Single ended input matching cell implementation. (c) Differential ended input matching cell.

5.3 Differential ended LNA architectures

A fully differential ended LNA architecture is shown in Fig. 8 where the first and the second stage of the single ended architecture have been duplicated. This way the fully differential LNA has similar electrical performances than the single ended LNA at the price of about twice the DC power consumption.

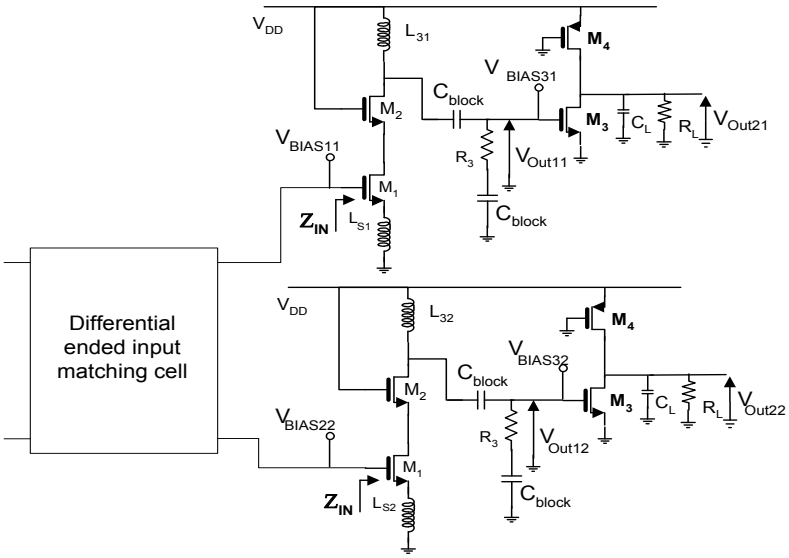

Fig. 8. Fully differential LNA architecture.

A differential ended termination at the LNA output can also be obtained by adding a third stage where a single to differential conversion is made as shown in Fig. 9. This way the inductor number needed is the same than in the single ended architecture and the whole LNA power consumption is nearly unchanged. Like for the second stage, the third stage voltage gain drop with the frequency must be compensated by setting the Q factor Q_3 of the first stage output load to the value that achieves a flat LNA amplification in the whole bandwidth.

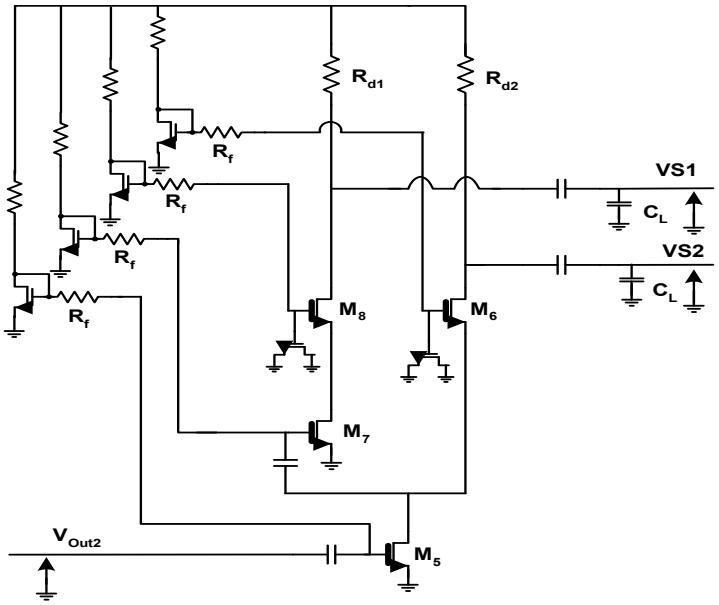

Fig. 9. Single ended to differential ended conversion stage.

6. LNA Implementation in Standard CMOS Technologies

6.1 Layout and simulation methodology

An implementation methodology of LC filter UWB LNA in a 0.13µm standard CMOS technology is given in this section (Battista et al., 2010). The technology consists of a high resistive substrate (about 10 Ωcm) with 6 metal layers, MIM capacitors and spiral inductors with RF models. Fig. 10 shows the microphotograph of a stand alone LNA prototype. Due to the large distances between inductors imposed by the technological design rules, long interconnects as long as 300µm are needed in the input matching cell. In such interconnects both the inductive, capacitive and resistive effects must be taken into account in simulation in order to optimize the layout. Additionally such interconnects must be properly designed to minimize the losses and so the noise figure. For theses purposes we used low characteristic impedance microstrip lines (MSL) designed according to the technological design rules. Generally, for MSL topology realized in CMOS technologies, ground is located on the lowest metal layer and the highest and thickest metal layer is used to design the signal path. CMOS foundry design kits don't usually contain transmission line models. To describe MSL, physical TEM T-Line model available in A.D.S. software has been used. This model provides an electrical description of frequency dependant loss in single mode quasi-TEM wave-guide. All parameters of the model are extracted from full wave Electromagnetic simulations.

The MSL ground plane, which is connected to the HF ground pads, is the local ground at the chip level. The power supply pad (VDD) is decoupled by using several MIM and MOS capacitors in order to get a large on chip capacitor value (a few hundred of pF) leading to a low return path ground impedance at high frequencies.

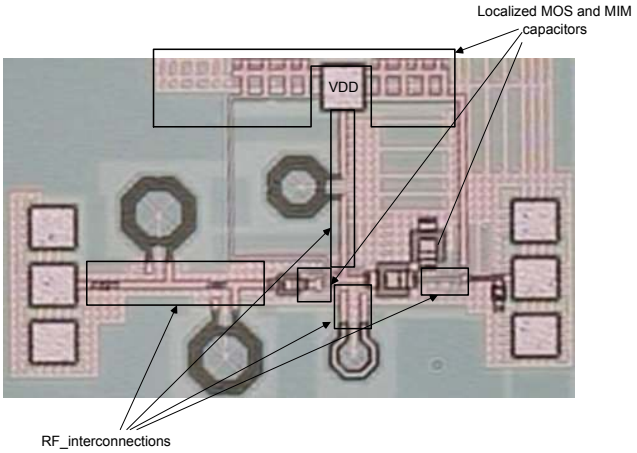

Fig. 10. Microphotograph of a stand alone LNA prototype.

For the LNA electrical simulations, we used the design kit models for active and passive lumped components, and the T-Line model, described above, for the MSL. MSL effects modify LNA performances, particularly the bandwidth and the cut-off frequencies. So to achieve the targeted characteristics, the initial component values must be modified according to the layout, by taking into account the interconnect effects. Fig. 11 shows a comparison between the measured input return loss and the simulation results with and without the MSL model. This comparison clearly shows that interconnects effects shift significantly the input matching cell bandwidth (about 1GHz in this case). By using MSL, both parasitic effects (inductive and capacitive effects) are well modelled and controlled, consequently the simulation results agree well with measurement results. Fig. 12 shows a comparison between measured and simulated results of the voltage gain and the noise figure for a 6.8-8.8 GHz LNA prototype. A good agreement between measured and simulated results is also observed.

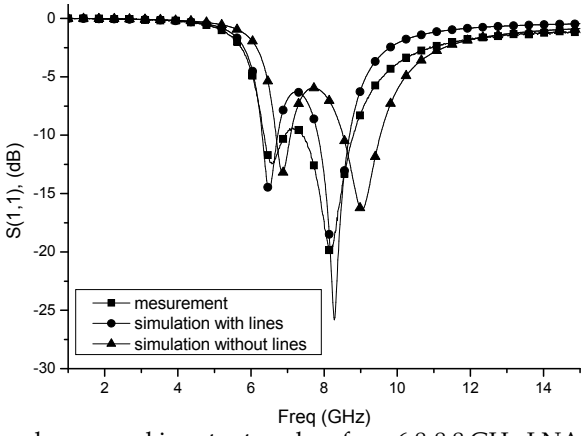

Fig. 11. Simulated and measured input return loss for a 6.8-8.8 GHz LNA.

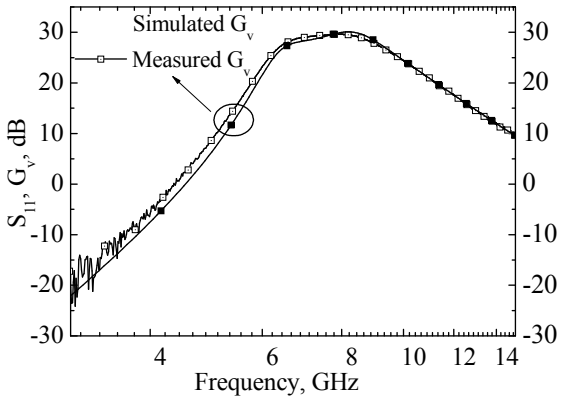

Fig. 12. Simulated and measured voltage gain loss for a 6.8-8.8 GHz LNA.

6.2 LNA implementation in UWB System on Chip

The methodology presented in section 6.1 has been validated on several stand alone LNA for different UWB sub-bands. These results are presented in section 7. Despite of the good agreement observed between simulation and measurement results in the case of simple test structures, UWB LNA can not be integrated into system-on-chip (SoC) without dealing with the substrate coupling effects when analog and digital circuits operate in a same chip. In this section the implementation of a LNA in an Impulse Radio UWB SoC is discussed. Fig. 13 shows a IR-UWB receiver architecture where the LNA is followed by a high speed ADC. In this example the ADC is built of D-latches, oscillators and buffers. Switching noise of such digital circuits generates harmonics that propagate through the silicon substrate and ground network and affect the sensitive analog HF circuits like LNA. Substrate noise effects are particularly important in UWB SoC where lower order harmonics fall in the large bandwidth of sensitive components like the LNA.

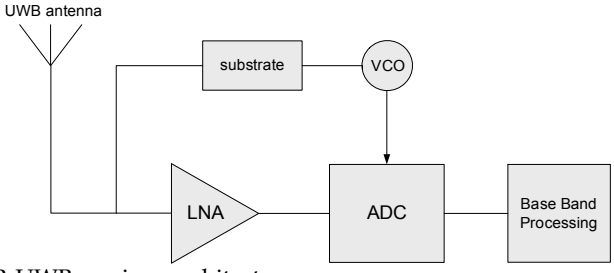

Fig. 13. Typical IR-UWB receiver architecture

Different devices that built the LNA can be affected by substrate noise. The active devices are less influenced thanks to the guard rings placed close to the transistors. However the large surface of ground shield of inductors can modify the path of noise propagation and inject the noise into the ground network of the chip. The noise received at LNA input may degrade significantly the receiver operation. Indeed the substrate noise is amplified by the

high voltage gain of the LNA and is sampled by the ADC. When efficient shielding and grounding techniques are not used high substrate noise level may be measured at the LNA input.

Guidelines to reduce the substrate noise in UWB SoC are given in (Fanei et al., 2007). The substrate noise can be decreased by reducing the VCO frequency, introducing a ground plane to protect sensitive interconnects (such in MSL case), or increasing the distance between sensitive analog and digital circuits.

Another way to reduce the substrate noise at the LNA input can be deduced from EM simulations which indicate that patterned ground shields of inductors inject substrate noise into the ground network. By separating the inductor ground shields from the ground circuit of the LNA, the substrate noise can be reduced in the UWB band. Fig. 14 shows the EM models of conventional and modified layouts of the LNA input matching cell and Figure 15 shows a comparison between the power spectrum of the two structures. The noise is injected through a metallic plane instead of a full VCO implementation (Fanei et al., 2007).

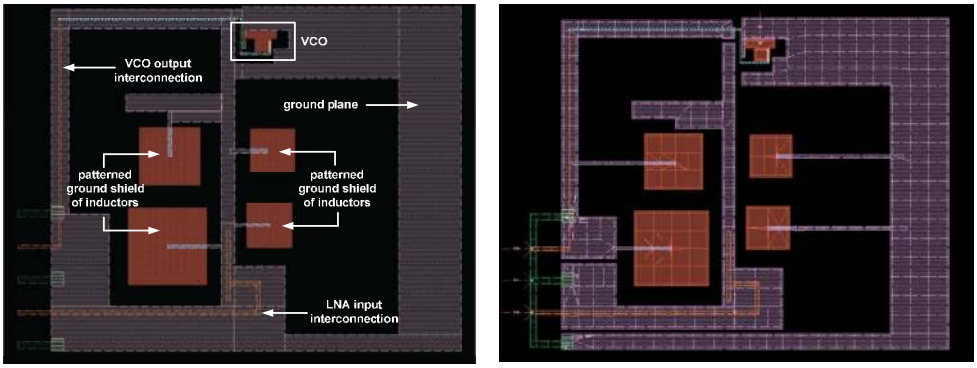

Fig. 14. (a) EM model of the interconnect of the IR-UWB receiver. (b) EM model of the modified layout.

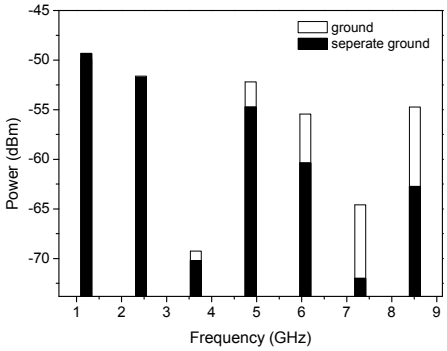

Fig. 15. Injected substrate noise spectrum at LNA input for the conventional and modified LNA layouts.

Simulations show that the LNA ground separation allows an injected substrate noise reduction in the UWB frequency band. The noise level reduction is around 5 to 10 dB in the 6-10 GHz frequency band.

6.3 LNA packaging

Regarding the LNA packaging stringent issues must be overcome to meet the signal integrity for UWB bandwidth and especially in the case of large bandwidth pulses. UWB is generally used for low cost applications and consequently high performance high end packages cannot be used. Low cost packages generally use bond wire interconnects, however the bandwidth of such interconnects is limited by the parasitic inductor coming from bond wire lengths. The schematic description of a high frequency bond wire carrier to die transition is given in Fig. 16.a. The transition generally connects a 50Ω grounded coplanar line on the chip carrier to on chip microstrip line. The transition includes three bond wires. The length of the bond wires with usual technological design rules for the die and package is about 1 mm. Such high frequency bond wire carrier to die transition can be modelled by an equivalent π network between two reference ports P1 and P2 (see Fig. 16.a) (Cubillo et al., 2008). It should be pointed that the bond wire transition model given in Fig.16.b includes the effects of both the signal bond wire and also the two bond wires connecting the carrier ground to the die ground. If a typical value of 15dB Return Loss is targeted in the bandwidth such basic transition cannot meet the 3.1-10.6 GHz UWB bandwidth.

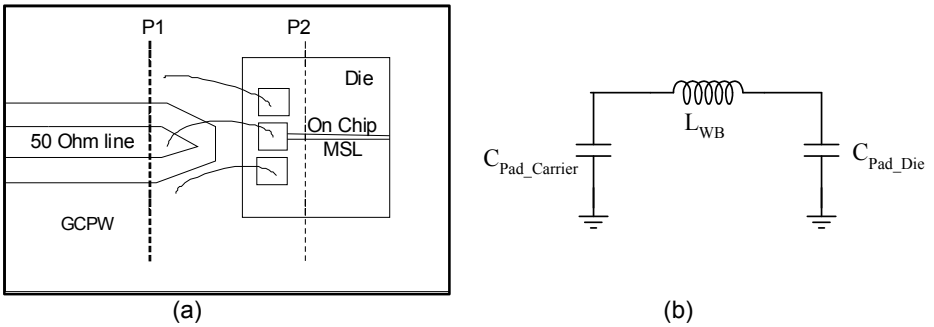

Fig. 16. Bond wire transition. (a) Schematic description. (b) Lumped equivalent π network.

The transition bandwidth can be extended up to 10.6 GHz by designing a third order low pass filter embedding the bond wire transition ensuring a ripple value lower than that of the wire bond transition himself (Cubillo et al., 2008). As shown in Fig. 17 the Low-Pass filter inductor is obtained thanks to the inductor of the π network of the bond wire transition model L_{WB}. The two capacitor of the Low-Pass filter are obtained by adding a distributed capacitor C_1 on the carrier and a MIM capacitor C_2 on the chip.

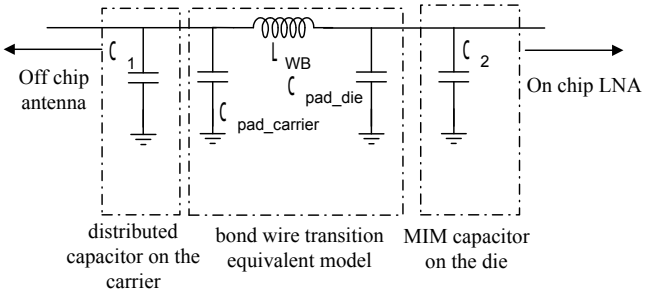

Fig. 17. Third order low pass filter embedding the bond wire transition.

7. Some results

Many LNA prototypes have been implemented in a standard 0.13µm CMOS technology. All the LNA outputs are loaded by a 60fF capacitor in order to emulate an ADC or a pulse detector load. The measurements instruments (spectrum analyser for the noise characterization and network analyser for scattering parameters measurements) are isolated at LNA output by using an on chip capacitance divider. For accurate characterization of the prototypes, the on chip capacitance divider has been also characterized on the same wafer to retrieve the output voltage from S parameters. The noise figure measurements are made with a spectrum analyzer and a noise source taking into account the mismatch at LNA output. The measurement results are summarized in Table 2 and compared to other published UWB LNAs.

	Tech. µm	**BW GHz**	**Area mm²**	**P_{DC} mW**	**Gain dB**	**NF dB**	**S_{11} dB**	**IIP3 dBm**
(Yu et al., 2007)	0.18	2.7-9.1	1.57	7	10	3.8-6.9	<-10	+1
(Heydari, 2007)	0.18	0.1-11	0.76	21.6	8	2.9	<-12	-3.5
(Chen, 2007)	0.18	2-11.5	0.33	13.4	14.8	3.1-4	<-10	+3
(Chen & Huang, 2007)	0.18	2.8-7.2	1.63	32	19.1	3-3.8	<-5	-1
(Reiha & Long, 2007)	0.13	3.1-10.6	0.87	9	15.1	2.1-2.8	<-10	-8.5
(Liao & Liu, 2007)	0.18	1.2-11.9	0.59	20	9.7	4.5-5.1	<-11	-6.2
(Shim et al., 2007)	0.18	0.4-10	0.42	12	12.4	4.4-6.5	<-10	-6
(Bevilacqua & Nikenejad, 2007)	0.18	2.9-11	0.98	9.5	16	3.8-4.4	<-10	-
This work	0.13	6.8-8.8 [1]	0.4	15	29.5 [3]	4-5.2	<-10	-8.5 [4]
This work [5]	0.13	6.8-8.8 [1]	0.5	21	30.6 [3]	-	<-7.8	-8 [4]
This work	0.13	6-10 [2]	0.4	21.6	26.5 [3]	3.5- 4.6	<-12	-8 [4]
This work [5]	0.13	6-10 [2]	0.5	22	28 [3]	-	< -8	-8 [4]
This work	0.13	3.1-10.6 [1]	0.4	18	22 [3]	2.8-3.7	<-10	-7 [4]
This work [4]	0.13	6.4-7.8 [1]	0.4	14	31 [3]	3.3-4.7	<-8	- 8
This work [4,5]	0.13	6.4-7.8 [1]	0.5	20	34 [3]	3.4-4.7	<-8	-8
This work [4,6]	0 .13	6.4-7.8 [1]	0.77	28	35 [3]	3.2-4.4	<-7	-
[1]1dB bandwidth ; [2] 0.5dB bandwidth ; [3] voltage gain ; [4] simulated value; [5]differential output,[6] fully differential								

Table 2. Summary of several published CMOS UWB LNA

8. Conclusion

The design of Ultra-Wide-Band LC filters LNA has been presented in this chapter. Architectures for both small fractional bandwidths such as the 6-8.5 GHz ECC frequency band and for large fractional bandwidths such as 3.1-10.6 GHz FCC frequency band have been proposed. Based on an analytical modelling of the LC filters LNA architecture, a design methodology allowing the noise figure minimization and the voltage gain maximization has been presented. The LNA implementation in standard CMOS technologies in the context of integrated receivers has been considered. Simple layout rules allowing reliable designs have been proposed. Several LNA prototypes for different fractional bandwidths have been fabricated in a 0.13µm CMOS technology. Measurement results agree well with the simulations and compare favourably with other published LNA.

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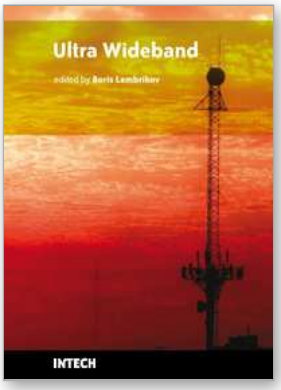

Ultra Wideband

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Ultra wideband technology is one of the most promising directions in the rapidly developing modern communications. Ultra wideband communication system applications include radars, wireless personal area networks, sensor networks, imaging systems and high precision positioning systems. Ultra wideband transmission is characterized by high data rate, availability of low-cost transceivers, low transmit power and low interference. The proposed book consisting of 19 chapters presents both the state-of-the-art and the latest achievements in ultra wideband communication system performance, design and components. The book is addressed to engineers and researchers who are interested in the wide range of topics related to ultra wideband communications.

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