Chapter 6

Silicon Epitaxial Reactor for Minimal Fab

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Additional information is available at the end of the chapter

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Abstract

Cost-effective and mass production of size-controlled wafers becomes one of the future trends for electronic devices. Herein, we design a Minimal Fab system for the growth of half-inch-diameter silicon wafer devices. Different from the conventional chemical vapour deposition (CVD) systems, a new-type of CVD reactor was designed and developed for the Minimal Fab. The minimal CVD reactor has a small reaction chamber for rapid growth processes. It employed (i) a vertical gas flow, (ii) heating modules using concentrated infrared light, (iii) chlorine trifluoride gas for quick reactor cleaning and (iv) optimized epitaxial growth conditions so that the reactor cleaning is not necessary. Reducing the total gas flow rate is an effective way to increase the wafer temperature. The heating process was further assisted by the absorption of infrared light by the precursor trichlorosilane. The slimly designed reflector could help in improving the heating speed.

Keywords: chemical vapour deposition, infrared light heating, reflectors, cleaning process

1. Introduction

The electronic device fabrication follows the two major trends, that is, the larger silicon wafer diameter and smaller design rule [1], mainly for economic reasons. A huge number of the device chips are produced in this manufacturing system. These trends require a huge investment for developing and preparing the plant.

However, we have the other technical trend [2] that the highly integrated device chips are customized and applied to various fields including the information technologies. For this purpose, a small amount of various chips are flexibly produced. Here, the Minimal Fab [3–6] is expected to flexibly produce just the right number of electronic device chips, from one to

million, on-demand and on-time, consuming less material and power. For this concept, a small silicon wafer having 12.5 mm diameter allows the great flexibility. It enables the very quick processes of the lithography, thin film formation, annealing and others. The instruments have a very small footprint. The chemical vapour deposition (CVD) process and its reactor should be developed as the key technology.

Ordinary CVD reactors used for epitaxial growth of large-diameter wafers consume a large amount of gases and heating power. For fast growth of small-scale devices, such as 12.5-mm wafer, Minimal Fab is designed better because a slow gas flow rate and slim heating modules are used. In addition, the environment inside the growth chamber is easily maintained and therefore the regular chamber cleaning for ordinary CVD reactors becomes less necessary for Minimal Fab. However, some parameters that are ignored in ordinary CVD systems may become effective in Minimal Fab. Special care should be paid to finely tune those important parameters.

To fabricate reactors for small substrates, the thermal condition becomes different when compared to that for the large substrates [7]. The concentrated infrared flux effectively heats the small substrate; the thermal process becomes very rapid. In addition to the heating system, the highly reactive gas of chlorine trifluoride (ClF_3) [8] is chosen for the reactor cleaning because it can easily remove the silicon film, unnecessarily formed in the CVD reactor, at various temperatures even at room temperature.

In Section 2 [9], a small footprint CVD reactor for producing silicon thin films is explained. This employs the technical issues of (i) vertical gas flow, (ii) a concentrated infrared flux and (iii) *in situ* reactor cleaning using chlorine trifluoride gas. Steps (i) and (ii) achieve a less heating energy and a rapid cooling. The cleaning process is rapid by (iii). The heating step is not necessary because the chlorine trifluoride gas is reactive even at room temperature. Section 3 explains the practical thermal condition [10, 11]. For achieving the rapid process, the infrared light absorption by the precursor gas is useful. Simultaneously, the cleaning-free process becomes possible. In Section 4, the heat transport near the wafer is evaluated [12]. The thin plates are recognized to be the suitable reflector material. For the quick temperature up and down, the reactor parts set near the wafer should be small, slim and thin. The wafer rotation and the highly heat-conductive susceptor help in achieving the symmetrical and uniform profile of silicon epitaxial film thickness.

2. Silicon chemical vapour deposition process for minimal fab

In this section, the CVD reactor was designed and developed, taking into account the thermal process using the reflector, which concentrates infrared flux. The reactor cleaning process using the highly reactive chlorine trifluoride gas is also employed.

2.1. Chemical reaction for silicon epitaxy

The chemical reactions at silicon substrate surfaces [13] are briefly shown as follows:

$$SiHCl_3 \rightarrow {}^*SiCl_2 + HCl\uparrow \qquad ({}^*\text{: Chemisorbed at surface}) \tag{1}$$

$${}^*SiCl_2 + H_2 \rightarrow {}^*Si + 2HCl\uparrow \tag{2}$$

Similar to the ordinary silicon epitaxial growth, trichlorosilane ($SiHCl_3$) is used in a hydrogen ambient. Firstly, trichlorosilane is chemisorbed at the surface to form the intermediate species, $*SiCl_2$. Next, it reacts with hydrogen to form silicon. Thus, the overall chemical reaction is written as follows:

$$SiHCl_3 + H_2 \rightarrow Si + 3HCl\uparrow \tag{3}$$

Assuming the Eley-Rideal model, the growth rate is expressed as follows:

$$\text{Growth rate} = \frac{k_{Ad}k_r[SiHCl_3][H_2]}{k_{Ad}[SiHCl_3] + k_r[H_2]}, \tag{4}$$

Where k_{Ad} and k_r are the rate constant for Eqs. (1) and (2), respectively. When k_{Ad} $[SiHCl_3]$ is significantly larger than k_r $[H_2]$, the epitaxial growth rate becomes as follows:

$$\text{Growth rate} = k_r[H_2] \tag{5}$$

Because the hydrogen concentration in the reactor is nearly constant, the epitaxial growth rate simply depends on the wafer temperature.

Generally, the epitaxial growth rate at 1100°C is about 1–4 μm/min by the ordinary horizontal cold wall reactor and is about 8 μm/min by the high-speed rotation vertical reactor.

In order to avoid the formation of surface defects, such as light point defects, the gas phase chemical reaction is suppressed by maintaining the gas phase temperature low, that is, by employing the cold wall environment.

2.2. Thermal condition

Figure 1 shows the heat transport for the silicon wafer in the minimal CVD reactor. The half-inch silicon wafer is heated by the infrared flux, Q_{IR}, emitted from the halogen lamps. The heat is emitted from the half-inch silicon wafer, Q_{Em}, as radiation heat. The gas flow containing the precursor gas from the gas nozzle takes the heat away from the wafer, Q_{Flow}.

By concentrating the infrared flux, Q_{IR} effectively reaches and locally heats the substrate with minimizing the heat loss. The distance between the silicon wafer and the gas nozzle can be changed by finely adjusting Q_{Flow}. In order to effectively heat the half-inch wafer, the half-inch wafer is placed below the reflector, as shown in **Figure 2(a)**. The half-inch silicon wafer is heated using the infrared flux coming from the upper outside.

By employing this geometry, Q_{Em} is high, because the emission of radiation heat is not disturbed. Although the Q_{Em} value decreases the wafer temperature, the increasing rate of the wafer temperature is high because of the high Q_{IR} value. Additionally, the cooling rate of the wafer becomes high.

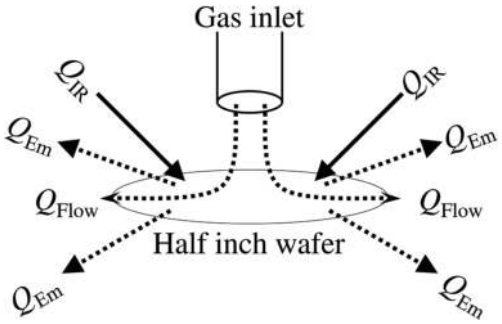

Figure 1. Heat transport for the silicon wafer in the minimal CVD reactor.

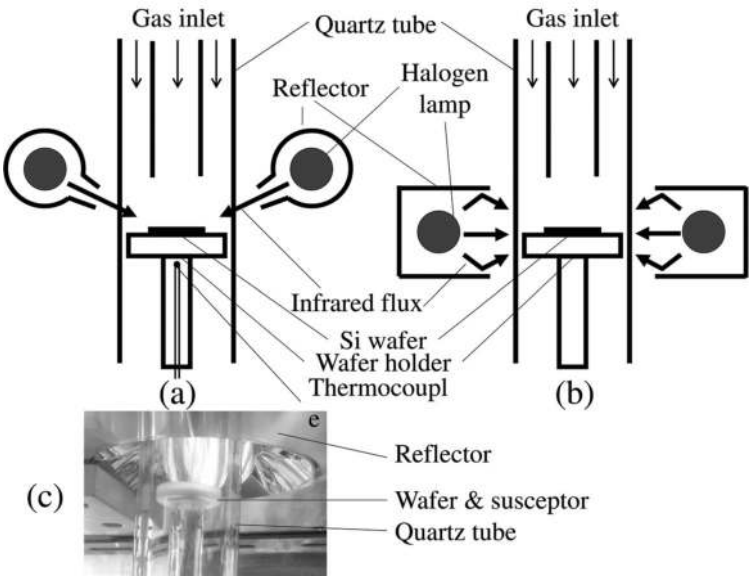

Figure 2. The minimal CVD reactor, (a) using the reflector concentrating the infrared flux to the silicon wafer, (b) using the ordinary type reflector, in which the silicon wafer is enclosed and (c) photograph of the minimal reactor.

2.3. Cleaning process

The reactor cleaning is necessary for removing the film produced around the substrate, such as at the wafer holder and the quartz tube. The typical silicon CVD process [14] utilizes hydrogen chloride gas near 1200°C. Such high-temperature process requires a long period for increasing and decreasing the temperature. By contrast, the chlorine trifluoride gas is useful, because the following chemical reaction occurs at any temperatures, even at room temperature [8],

$$3Si + 4ClF_3 \rightarrow 3SiF_4\uparrow + 2Cl_2\uparrow \tag{6}$$

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2.4. Reactor

Figure 2(a) shows the reactor, which consists of a quartz tube (inner diameter of 24 mm), a quartz wafer holder, gas inlets, three halogen lamps, and a reflector. A half-inch silicon wafer is set on the quartz wafer holder. The inner zone and the outer zone gas inlets have diameters of 7 and 24 mm, respectively. A half of the total gas was introduced to each of the inlets. The distance between the silicon wafer and the bottom of the inner zone gas inlet was 3 cm, in this section. **Figure 2(c)** shows a photograph which depicts the half-inch silicon wafer heated by the infrared flux.

Figure 2(b) shows the CVD reactor having an ordinary type reflector. The half-inch silicon wafer is enclosed in the reflector. The infrared flux approaches *via* the various paths experiencing multiple reflections by the reflector. Comparing this with the minimal CVD reactor, the half-inch wafer cooling rate is shown to be influenced by the reflector geometry. This will be explained in detail in Section 2.6.

The wafer temperature is measured in ambient nitrogen by an R-type thermocouple, directly attached to the backside of the half-inch silicon wafer. During the silicon film deposition in ambient hydrogen, the thermocouple is placed in the quartz wafer holder, as shown in **Figure 2(a)**.

2.5. Process

For the silicon film formation, the carrier gas and precursor gas are vertically introduced to the silicon wafer. The carrier gas is hydrogen (H_2) and the precursor gas is trichlorosilane. The cleaning gas is chlorine trifluoride diluted to 5% in ambient nitrogen at atmospheric pressure. The total gas flow rate is 0.2–1.2 slm. The half-inch silicon wafer is heated to 800–1100°C.

The silicon CVD process is shown in **Figure 3**. After the silicon wafer is heated, the trichlorosilane gas is introduced for the silicon deposition. After terminating the trichlorosilane gas supply, the wafer is cooled down and unloaded from the reactor. The chlorine trifluoride gas is introduced into the reactor at atmospheric pressure and at room temperature for

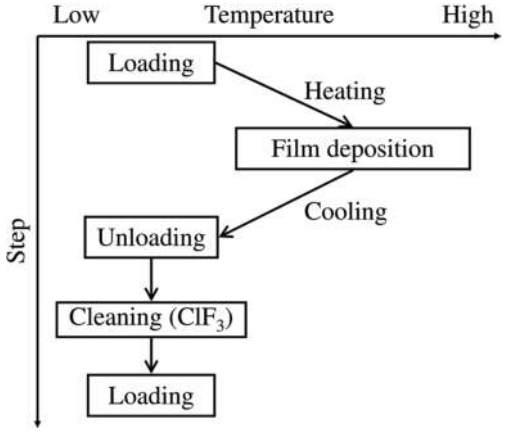

Figure 3. Silicon chemical vapour deposition process for the Minimal Fab.

removing the silicon film formed on various places in the reactor. The flow rate of nitrogen and chlorine trifluoride gas is 1 and 0.05 slm, respectively.

2.6. Cooling rate

The capability of the reflector is first evaluated by the cooling rate of the half-inch silicon wafer. **Figure 4** shows the cooling rate of the minimal CVD reactor at the nitrogen flow rate of 1 slm, using the reflectors of minimal and ordinary type, shown in **Figure 2(a)** and **(b)**, respectively. **Figure 4** shows the decreasing temperatures of the half-inch wafer. The cooling rate of the minimal CVD reactor is −22 K/s, which is 20% greater than that using the ordinary-type reflector.

2.7. Heat balance

The electric power for heating the silicon wafer is evaluated with adjusting the gas flow rate and the trichlorosilane gas concentration. The half-inch wafer temperature is obtained following the relationship between the temperatures on the backside of the half-inch wafer and the temperature below the quartz wafer holder measured by thermocouple. Additionally, based on the silicon film growth rate saturation [13] at temperatures lower than 1000°C and at the high trichlorosilane gas concentrations, the half-inch wafer temperature is obtained.

The half-inch wafer temperature in a steady state is influenced by various conditions, such as the lamp voltage, V (V), the total gas flow rate, F_{TotalGas} (sccm) and the trichlorosilane gas concentration, C_{TCS} (%). Using a least-squares approximation, the half-inch wafer temperature, T_{Wafer} (°C), is obtained, assuming that each parameter linearly influences the T_{Wafer} value.

$$T_{\mathrm{wafer}}(^{\circ}\mathrm{C}) = 90\sqrt{V(V)} - 0.13F_{\mathrm{TotalGas}}(\mathrm{sccm}) - 4.3C_{\mathrm{TCS}}(\%) + 310(^{\circ}\mathrm{C}) \tag{7}$$

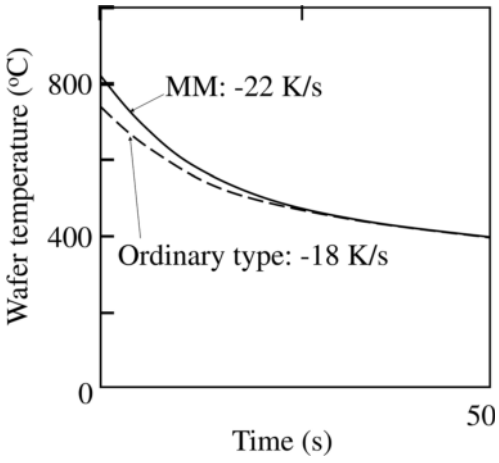

Figure 4. Cooling rate of half-inch silicon wafer in the minimal CVD reactor and the reactor using the ordinary type reflector. (In ambient nitrogen: 1 slm and atmospheric pressure.).

The T_{Wafer} value increases by the increasing V value and decreases by the increasing $F_{TotalGas}$ value and C_{TCS} value. Particularly, the increase in $F_{TotalGas}$ of 10 sccm and that of C_{TCS} of 0.25% induces a 1°C decrease in T_{Wafer}.

Following Eq. (7), the half-inch wafer temperature is estimated as a function of the lamp voltage and the total gas flow rate at the trichlorosilane concentration fixed to be 3.5%, as shown in **Figure 5**. Eq (7) shows that the lamp voltage becomes 10–20 V lower by decreasing the total gas flow rate.

2.8. Reactor cleaning

As shown in **Figure 6(a)**, a polysilicon film is formed on the wafer holder and on the inner wall of the quartz tube during the film deposition. The thick silicon film is formed at a height near that of the half-inch silicon wafer, because the reactor inner wall near the substrate is high.

Because the film on the quartz wall might produce particles to cause surface defects, it must be removed. Thus, chlorine trifluoride gas [2] at 5% is introduced into the reactor at room temperature in the ambient nitrogen. **Figure 6(b)** shows a reactor before introducing the chlorine trifluoride gas. **Figure 6(c)** shows that the silicon film on the right half of the reactor wall was removed after 1 min. The right half of the wafer holder is clearly observed. Although the silicon film on the left half of the reactor wall reduces, a thick film still remains.

As shown in **Figure 6(d)**, only a small amount of the polysilicon film remains after 2 min on the left position of the reactor wall. After 3 min, the polysilicon film is perfectly removed, as shown in **Figure 6(e)** which clearly gives an image of the entire wafer holder. The polysilicon film formed on the inner wall of the quartz tube is quickly and perfectly removed at room temperature.

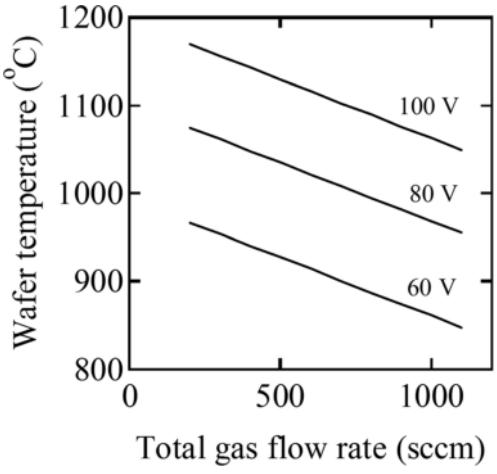

Figure 5. Wafer temperature changing with the lamp voltage and the total gas flow rate.

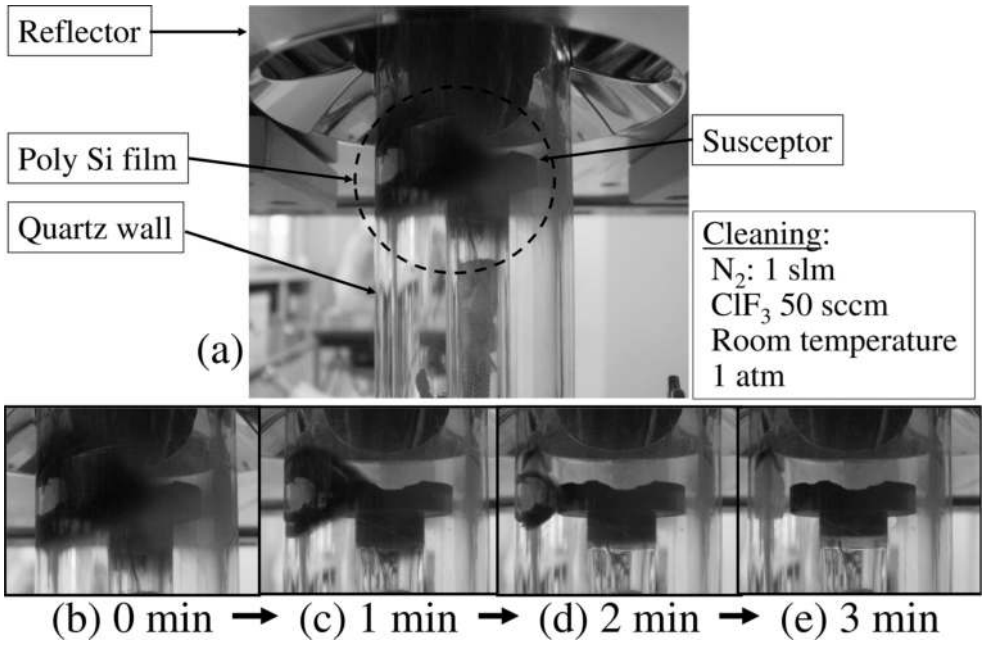

Figure 6. Reactor appearance along the reactor cleaning at room temperature. (a) After the film deposition; (b–e): the decrease of poly Si film.

3. Thermal condition

The wafer temperature is influenced by many parameters [9] of lamp voltage, total gas flow rate and trichlorosilane gas concentration. The details of these thermal influences are evaluated. Particularly, the light absorption and the heat transport by the gases are the major issues. **Table 1** shows the experimental conditions.

3.1. Temperature change caused by trichlorosilane

Figure 7 shows the quartz wafer holder temperature. The hydrogen and trichlorosilane flow rate are 220 and 12 sccm, respectively. The wafer holder temperature slowly becomes 568°C in the ambient consisting of only hydrogen, as shown using dark squares. When the trichlorosilane gas is added from 9 to 13 min, the wafer holder temperature increases, as shown using white squares, and reaches 609°C. Empirically, the wafer surface temperature increase by the trichlorosilane gas is *c.a.* 80 K.

Trichlorosilane has the infrared light absorption [15] at 3.3 and 2.2 μm. The halogen lamp emits the light near 1 μm, the wavelength of which widely distributes [16] to that longer than 2 μm. Thus, the trichlorosilane considerably absorbs the infrared light from the halogen lamps; it increases the temperature of the gas phase.

Parameters	Value
Pressure	Atmospheric pressure
Hydrogen gas flow rate	100–1000 sccm
Trichlorosilane gas flow rate	2–60 sccm
Chlorine trifluoride gas flow rate	50 sccm
Substrate	12.5 mm diameter silicon wafer
Electric power	55–100 V
Deposition time	1 min × n times or n minutes once
Substrate temperature	800–1000°C

Table 1. Silicon CVD conditions.

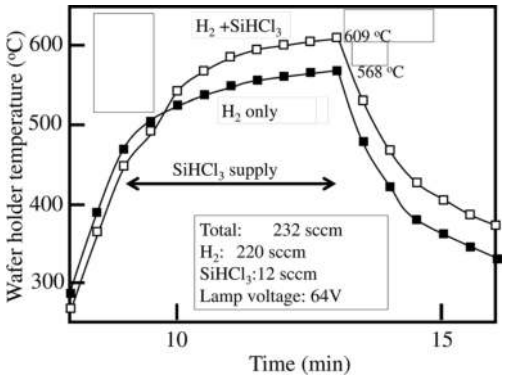

Figure 7. Temperature shift cause by $SiHCl_3$ supply for 4 min (at 64 V).

3.2. Influence of total gas flow rate

Figure 8 shows the wafer holder temperature during the silicon deposition. Dark squares are the temperatures at the hydrogen and trichlorosilane flow rate of 220 and 12 sccm, respectively. The wafer holder temperature increases from 8 min; the temperature increase becomes faster after the addition of trichlorosilane at 10 min. The wafer holder temperature reaches 588°C. The temperatures at the hydrogen and trichlorosilane flow rate of 165 and 9 sccm, respectively, are shown by white squares. The wafer holder temperature reaches 626°C which is higher than that at the higher gas flow rate. The wafer holder temperature increases with the decreasing total gas flow rate.

Although **Figure 7** might show that the decrease in the trichlorosilane gas flow rate induces the temperature decrease by means of less infrared absorption, the wafer holder temperature is actually increased. It is due to the heat transport by the gas flow [9].

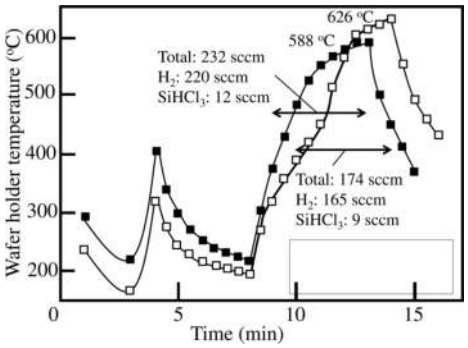

Figure 8. Temperature increase by the decreasing H_2 flow rate (at 65 V).

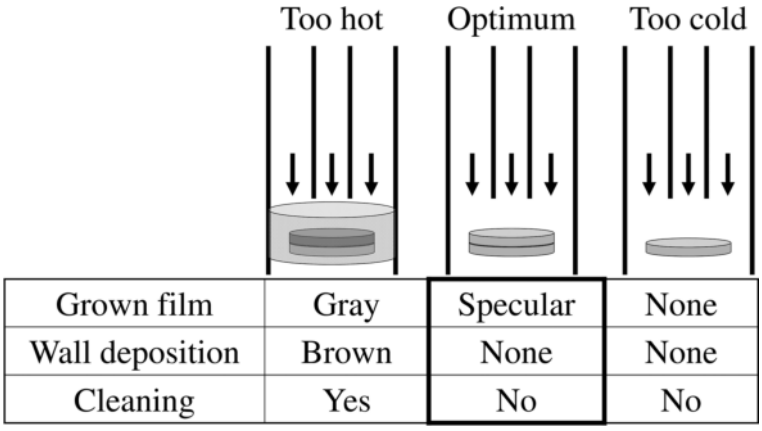

Figure 9. Film growth and wall deposition.

3.3. Temperature and obtained film surface

Figure 9 shows the relationship between the wafer temperature, the film surface and the quartz wall deposition. At a very high temperature, the silicon film deposition occurs at the silicon wafer surface and the quartz tube inner wall surface. The optimum temperatures produce the specular silicon epitaxial film without the tube wall deposition.

4. Reflector influence on rapid heating

In order to achieve the uniform-thick epitaxial film, the thermal conditions are important. The important issues are the infrared ray reflection design [7] and the heat transport through the reflectors set around the wafer. The CVD reactor for the large-diameter wafer has the large infrared lamp module consisting of large and thick reflector plates [9–11]. The reflector surface

not only concentrates the infrared rays to the wafer surface but also absorbs the heat coming from the lamps. Then, the reflector becomes high temperature. Through the reflector, various parts and the gas phase, the heat absorbed by the reflector is slowly conducted to the wafer. The temperature of reflector surface and wafer gradually increases during reaching the thermal steady state. Particularly, the massive metallic parts require long time for reaching a thermal steady state. In this case, the heating process requires more electric power and finer heat distribution control. In order to design a quick heat transport through the reflector maintaining low electric power, a thin and slim reflector is expected. The reflector geometry should be optimized for the minimal CVD reactor.

Infrared rays tend to converge to generate a hot spot [7]. For broadening the locally formed heat profile, a silicon carbide susceptor having high heat conductivity is convenient. Additionally, the wafer rotation is popular and effective for averaging the temperature distribution and the film growth rate [17].

In this section for achieving a quick thermal process, the heating behaviour is evaluated using two types of reflectors, that is, the Type-I reflector made of thick mirror plates used in the previous sections and the Type-II reflector made of thin plates. Additionally, the roles of the wafer rotation and the silicon carbide susceptor are explained for preparing a uniformly thick silicon epitaxial film.

4.1. Reactor and reflector design

Figure 10 shows the detail of minimal CVD reactor. Similar to the previous sections, the reactor has the inner and the outer inlet. The distance between the wafer and the inner inlet is 51–56 mm. In this section for improving the heat conduction, the silicon carbide plates are inserted beneath the wafer.

Figure 11 shows the Type-I and Type-II reflectors covered with an electroplated gold film. Three reflectors are horizontally arranged around the quartz tube, as shown in **Figure 10**. **Figure 11(a)** shows the Type-I reflector, which is evaluated in the previous sections. The main body of the Type-I reflector is a 50-mm-thick mirror plate. Its thick body maintains the temperature stable during the long process, because it is not sensitive to fluctuations in the temperature around the reactor. However, it may result in slow heat conduction through it.

As shown in **Figure 12(a)** and **(b)**, through the Type-I reflector and the Type-II reflector, respectively, the heat from the halogen lamps is transported to the silicon wafer. The solid lines indicate the heat conduction from the lamp to the reflector plate. This heat conduction also heats the wafer, with the radiation heat indicated by the dotted lines. Because the heat conduction requires long period to reach long distance, the large and thick Type-I reflector slowly achieves the steady state and makes the thermal process slow and long.

The Type-II reflector is shown in **Figure 11(b)**. This reflector consists of a 5-mm-thick plate which is significantly thinner than that of the Type-I reflector. This thin plate makes the heat transport through itself quicker than that of the Type-I reflector. Particularly, the temperature difference between the inside and outside of the reflector plate is reduced. The thermal process by the Type-II reflector can be quicker than that of the Type-I reflector.

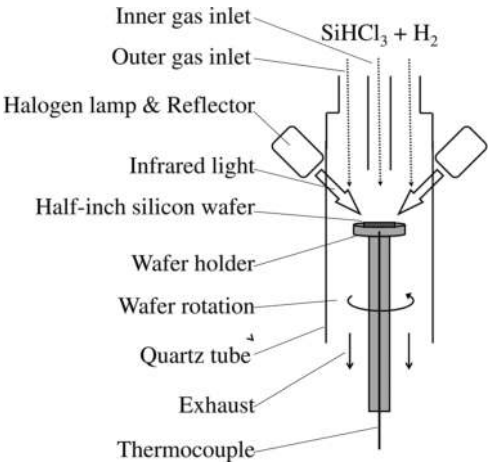

Figure 10. Half-inch silicon CVD reactor for the Minimal Fab.

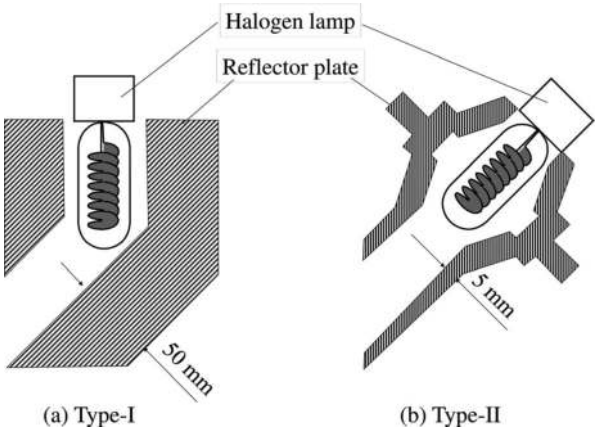

Figure 11. Two reflectors of (a) Type-I and (b) Type-II.

4.2. Process

The gas mixture of hydrogen (H_2) and trichlorosilane ($SiHCl_3$, TCS) is vertically introduced to the silicon wafer in ambient hydrogen at atmospheric pressure, as shown in **Figure 10**. The gas flow rates of the H_2 and TCS are 215 and 9 sccm, respectively. The electric power of 55–65 V is supplied to the halogen lamps. The total electric power is less than 1500 W.

Typically, the epitaxial film formation process has two major steps. Step A removes the native oxide film on the silicon wafer surface at 1100°C for 1 min. Next, the wafer temperature is

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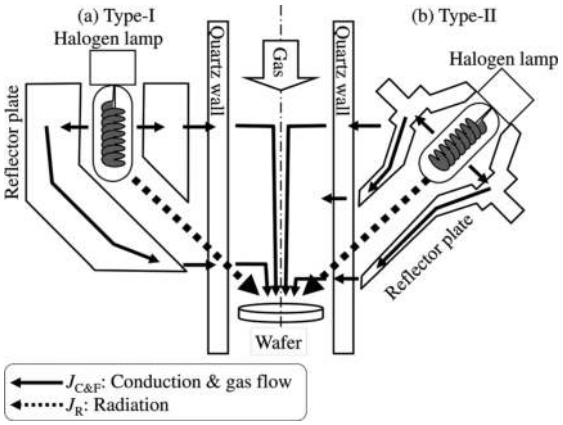

Figure 12. Heat transport from halogen lamp to silicon wafer through (a) Type-I and (b) Type-II reflectors. Dotted lines: heat transport by radiation; solid lines: heat transport by conduction and gas flow.

adjusted to 700–1000°C for Step B, forming the silicon epitaxial film for several minutes by the chemical reaction [13] following Eq. (3).

The process shown in **Figure 13(a)** has the stand-by step, Step C, between Step A and Step B. Step C, waiting for Step B after Step A, realizes the parallel process. The two virtual reactors, the A and B Reactors, are arranged for Steps A and B, respectively. Step C transports the wafer from the A Reactor to the B Reactor at low temperatures. Although the additional period is necessary for increasing and decreasing the temperature, Steps A and B can be simultaneously performed. The parallel process of Steps A and B is expected to become quicker. Thus, in the first part, Step C is intentionally performed using the Type-I and -II reflectors, in order to

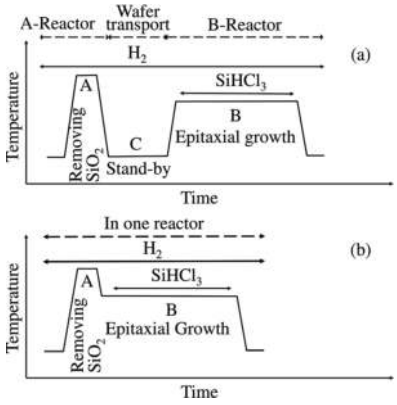

Figure 13. Process of silicon epitaxial growth by (a) Steps A–C and by (b) Steps A and B. Step A removes native oxide film, Step B forms silicon epitaxial film and Step C is for stand-by. Dotted lines show virtual reactor process.

compare their thermal behaviours through exactly the same process. In the second part, the effect of Step C was evaluated.

4.3. Wafer rotation and susceptor

For obtaining the uniform-thick epitaxial film by the classical ways [18], the wafer rotation and the silicon carbide susceptor are employed, as shown in **Figure 14**. Because even the slow wafer rotation has the effect of averaging the film growth rate along the concentric circle [17], the epitaxial film thickness is expected to become flat over the wafer. Silicon carbide has a high thermal conductivity [19] for decreasing the temperature difference over the wafer. The diameter and the thickness of the silicon carbide plate are 16 and 0.58 mm, respectively. Three silicon carbide plates are stacked beneath the silicon wafer.

4.4. Wafer temperature evaluation

The wafer holder temperature, T_{WH}, is measured and evaluated. The silicon wafer temperature, T_W, is obtained from the silicon epitaxial growth rate. At the wafer temperature lower than 1000°C and at the TCS gas concentration higher than 1%, the silicon epitaxial growth rate is governed by the surface chemical reaction. The epitaxial growth rate is expressed using the wafer temperature, T_W, [13]

$$\text{Growth rate } (\mu\text{m/min}) = 1.95 \times 109\, e^{(-26100/T_W)} \qquad (T_W < 1000^{\circ}\text{C}). \tag{8}$$

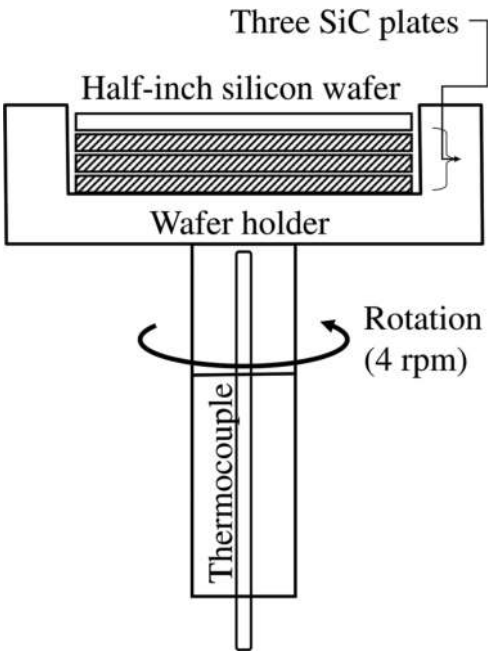

Figure 14. Half-inch wafer and silicon carbide susceptor on rotating wafer holder.

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When the wafer holder temperature, T_{WH}, is 650°C, the silicon epitaxial film growth rate was about 1.2 μm/min, corresponding to the T_W value near 960°C.

The silicon epitaxial film is formed by the two types of reflectors, as shown in **Figure 15**. The gas flow rates of the TCS and the H_2 were 9 and 215 sccm, respectively. Step C is intentionally introduced for cooling the reflector and for comparing the two types of reflector through the same process. In **Figure 15**, the dotted line and the solid line show the wafer holder temperatures during Step B immediately after Step C, by the Type-I and -II reflectors, respectively.

For the Type-I reflector, the TCS gas is introduced between 0 and 5 min. The wafer holder temperature finally becomes 573°C at 5 min at the halogen lamp voltage of 63 V. The solid line shows the temperature change using the Type-II reflector. The wafer holder temperature reaches 621°C at 4 min at the halogen lamp voltage of 62 V. The Type-II reflector can achieve the wafer temperature higher and faster than the Type-I reflector do.

The wafer holder temperature using the Type-I reflector still increases at 5 min as shown in **Figure 15**. As shown by the dotted line in **Figure 16**, the wafer holder temperature using the Type-I reflector at the halogen lamp voltage of 62 V can reach 553°C at 10 min. This is 70°C lower than that by the Type-II reflector. Additionally, the temperature using the Type-I reflector is entirely lower than that of Type-II through Steps A–C. Thus, the Type-II reflector achieves a quicker heating process.

In **Figures 15** and **16**, the wafer holder temperature increases after introducing the TCS gas at Step B. Because TCS gas absorbs the infrared light [15, 16], the gas phase temperature increases and finally the wafer temperature increases.

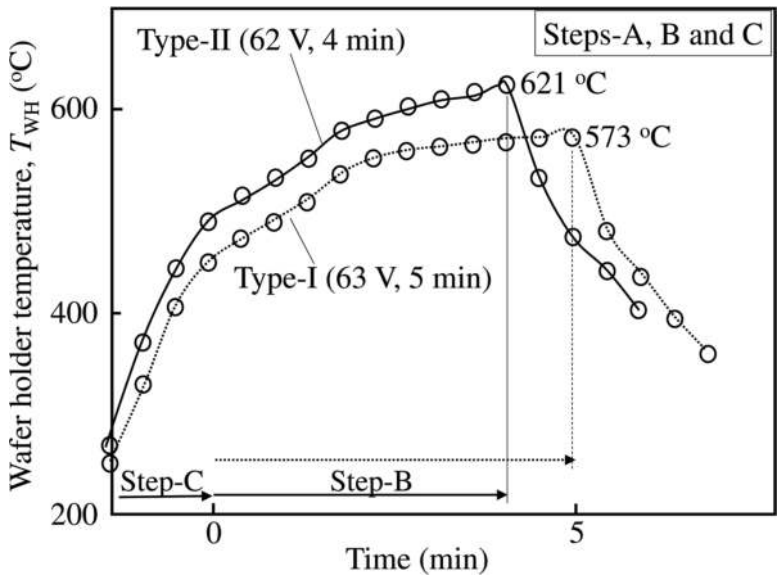

Figure 15. Temperature of wafer holder during Step B immediately after Step C. Dotted line: Type-I reflector at 63 V for 5 min and solid line: Type-II reflector at 62 V for 4 min.

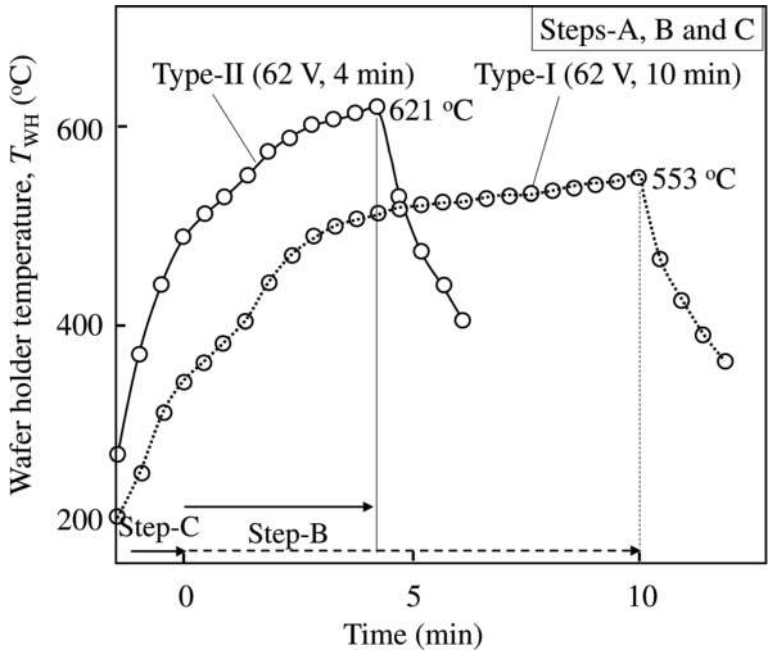

Figure 16. Temperature of wafer holder during Step B after Step C. Dotted line by Type-I reflector at 62 V for 10 min. Solid line by Type-II reflector at 62 V for 4 min.

For the thermal process optimization, the influence of Step C on the wafer temperature is evaluated using the Type-II reflector. **Figure 17** shows the wafer holder temperature with and without Step C at the halogen lamp voltage of 62 V. The flow rates of H_2 gas and TCS gas are 215 and 9 sccm, respectively.

The dotted line shows the wafer holder temperature through Steps A, C and B. In Step A, the wafer holder temperature reaches 650°C. During Step C, the wafer holder temperature is cooled to about 250°C, by decreasing the halogen lamp voltage to 30 from 80 V. The wafer holder temperature is then increased in Step B. At the halogen lamp voltage of 62 V, the wafer holder temperature becomes 621°C at 14 min. However, the wafer holder temperature still increases even at 14 min.

The solid line shows the wafer holder temperature during Steps A and B without Step C. The temperature during Step A is the same as the dotted line. After Step A, the halogen lamp voltage is increased to 62 V. The wafer holder temperature reaches 618°C at 6 min in a steady state. Thus, the process deleting Step C can be quick and stable.

4.5. Wafer rotation and susceptor

Using the Type-II reflector, the silicon epitaxial film is formed on the half-inch silicon wafer surface, by Steps A and B. The TCS and H_2 flow rates are 9 and 215 sccm, respectively, for 4 min.

http://dx.doi.org/10.5772/intechopen.69986

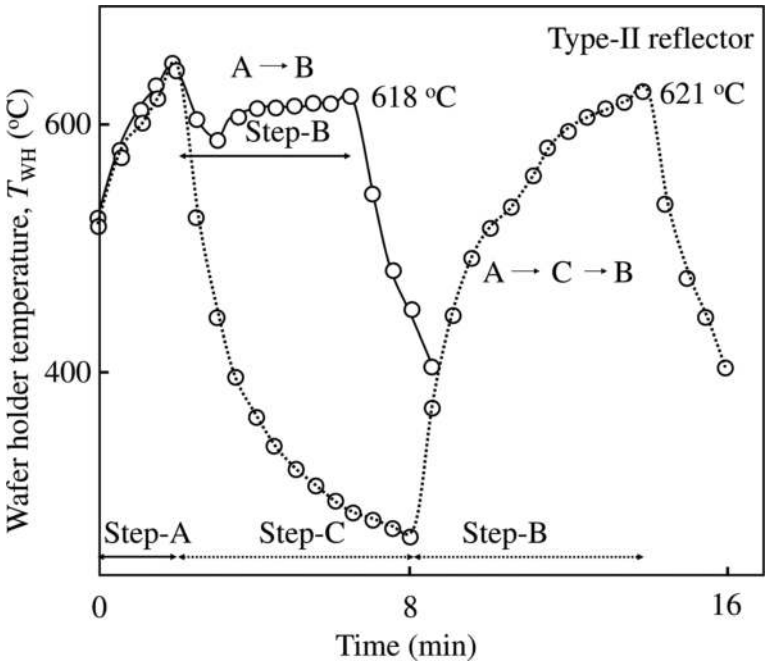

Figure 17. Wafer holder temperature using Type-II reflector. Dotted line: along Steps A, C and B and solid line: along Steps A and B without Step C.

The halogen lamp voltage at Step B is 60 V. The film thickness distribution is evaluated at five points along the longitudinal and transverse lines, using the dotted line and the solid line, respectively, as shown in **Figure 18**. **Figure 18(a)** shows the thickness profile of the epitaxial film which is formed without using the wafer rotation and without using the silicon carbide susceptor. The epitaxial film thickness along the *x*-axis is from 1.5 to 3.5 μm. By contrast, the epitaxial film thickness along the *y*-axis is very flat. In this figure, the film thickness shows a decrease from right to left. The epitaxial growth rate is near 0.5 μm/min, which corresponds to the wafer temperature of 950°C following Eq. (4). The epitaxial growth rate in **Figure 18** is governed by the rate of surface chemical reaction [13]. By the relationship, obtained in Section 2 [9], the introduced gas reaches the wafer surface and decreases its temperature. As shown in **Figure 19(a)**, by the asymmetric gas flow direction, the surface temperature is low in the left region. Corresponding to this temperature trend, the epitaxial film in the left region is thinner than that in the right region. Additionally, when the wafer is directly loaded on the quartz wafer holder, an adiabatic-like environment is formed. It produces a locally high-temperature region and the non-uniform thick film, because the infrared rays are easily concentrated to a local spot [20].

The wafer rotation is used for adjusting the asymmetric condition. **Figure 18(b)** shows the epitaxial film thickness profile, when the wafer rotates. The epitaxial film thickness shows a hill and a valley along the *x*- and *y*-axes. Although the thickness profile is averaged along the concentric circle of the rotating wafer, rather the complicated thickness profile appears. The

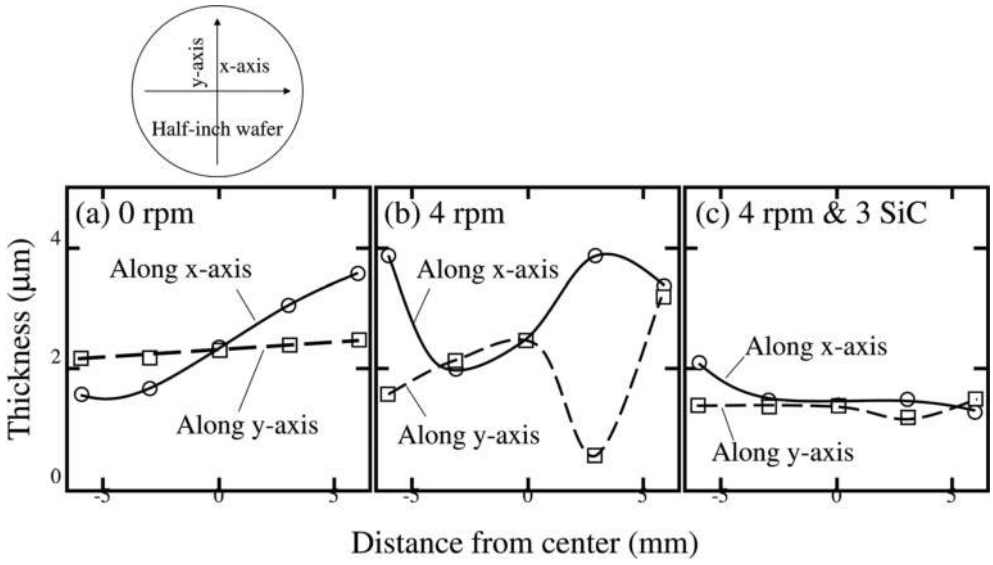

Figure 18. Thickness profile of obtained silicon epitaxial film: (a) without wafer rotation and without silicon carbide susceptor, (b) with wafer rotation and without silicon carbide susceptor and (c) with wafer rotation and with three silicon carbide susceptors.

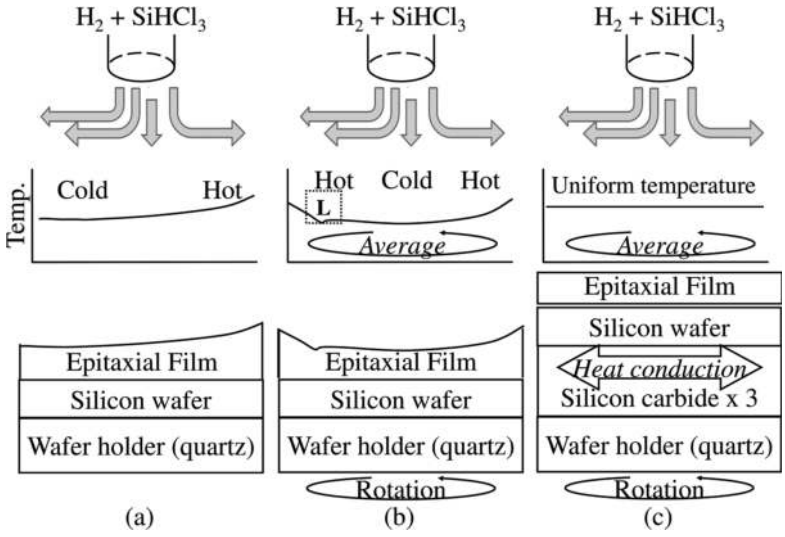

Figure 19. Influence of gas flow from the inlet, wafer rotation and silicon carbide susceptor on the epitaxial film thickness (a) with no wafer rotation and no silicon carbide susceptor, (b) with wafer rotation and no silicon carbide susceptor and (c) with wafer rotation and three silicon carbide susceptors.

local low- or high-temperature spot, denoted by the letter L, still remains. An additional method is necessary for obtaining the flat silicon film.

The locally high and low temperatures over the wafer surface may be produced due to the quartz material having a low thermal conductivity [20]. The heat transport in the horizontal direction is enhanced by the silicon carbide susceptor. **Figure 19(c)** shows that the local non-uniformity of the wafer temperature remaining even using the wafer rotation is reduced by the high heat transport through the silicon carbide susceptor. As shown in **Figure 18(c)**, the epitaxial film thickness becomes very flat along the *x*- and *y*-axes.

By using the small, thin and simple geometry of the reactor parts, the quick and flat epitaxial film production is possible. This concept is valid not only for the minimal CVD reactor.

5. Summary

A chemical vapour deposition reactor for the growth of half-inch silicon wafers is designed by employing (i) a vertical gas flow, (ii) rapid thermal operation using concentrated infrared light and (iii) a quick reactor cleaning process. For the rapid heating process, absorption of infrared light and heat transport by the flowing gases are active parameters. Under the optimized conditions, the cleaning-free process is possible. The reactor parts placed near the wafer must be small, slim and thin for quickly heating the wafer. The wafer rotation and the heat-conductive susceptor help to fabricate uniform silicon epitaxial films. Overall, important parameters are listed in **Table 2**. This table includes several parameters which are active and useful for the small-sized reactor.

Parameters	Value
Substrate	12.5 mm diameter silicon wafer
Gas flow	Vertical (from top to bottom)
Pressure	Atmospheric pressure
Precursor	Trichlorosilane ($SiHCl_3$)
Hydrogen gas flow rate	Less than 200 sccm
Trichlorosilane gas flow rate	20 sccm
Chlorine trifluoride gas flow rate (Reactor cleaning)	50 sccm in 1000 sccm in N_2
Heating module	Concentrated infrared light (Three halogen lamps) Slim and thin reflector
Electric power	55–65 V, less than 1500 W
Substrate surface cleaning	Near 1000°C in H_2 within 1 min
Deposition time	1–8 min
Substrate temperature	800–1000°C
Substrate rotation	4 rpm

Parameters	Value
Susceptor	Silicon carbide plate
Footprint	30 × 45 cm

Table 2. List of parameters: silicon epitaxial growth for Minimal Fab.

	Minimal CVD reactor	Ordinary CVD reactor
Wafer diameter	12.5 mm, single wafer	150, 200, 300 and 450 mm, multi-(batch) and single wafer
Total gas flow rate	<0.2 slm	>100 slm
Growth rate	Near 1 μm/min	1–8 μm/min
Pressure	1 atm (or reduced pressure)	1 atm or reduced pressure
Precursor	$SiHCl_3$	$SiHCl_3$, SiH_2Cl_2, SiH_4, and so on
Reactor cleaning	ClF_3 gas at higher than RT	HCl gas near 1200°C
Gas flow	Natural convection, Vertical (downward)	Forced flow, Vertical (downward), horizontal, cylinder, pancake, and so on
Heating method	Concentrated light by lamp heating	Lamp, resistant and inductive heating
Electric power	<1500 W	>100,000 W
Footprint	0.3 × 0.45 m^2	Several × Several m^2
Throughput	Several tens wafers/min (Target)	Several wafers/min
Reactor price	> $30,000 (Target)	> $3,000,000

Table 3. Comparison between minimal and ordinary CVD reactor.

The differences of the reactor design between the Minimal Fab and the ordinary CVD are listed in **Table 3**. The film growth on a small wafer using small gas flow rates significantly reduces system cost.

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