Chapter

# Semiconductor Epitaxial Crystal Growth: Silicon Nanowires

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## Abstract

The topic of nanowires is one of the subjects of technological rapid-progress research. This chapter reviews the experimental work and the advancement of nanowires technology since the past decade, with more focus on the recent work. Nanowires can be grown from several materials including semiconductors, such as silicon. Silicon is a semiconductor material with a very technological importance, reflected by the huge number of publications. Nanowires made of silicon are of particular technological importance, in addition to their nanomorphology-related applications. A detailed description of the first successfully reported Vapor–Liquid–Solid (VLS) 1-D growth of silicon crystals is presented. The bottom-up approach, the supersaturation in a three-phase system, and the nucleation at the Chemical Vapor Deposition (CVD) processes are discussed with more focus on silicon. Positional assembly of nanowires using the current available techniques, including Nanoscale Chemical Templating (NCT), can be considered as the key part of this chapter for advanced applications. Several applied and conceptional methods of developing the available technologies using nanowires are included, such as Atomic Force Microscopy (AFM) and photovoltaic (PV) cells, and more are explained. The final section of this chapter is devoted to the future trend in nanowires research, where it is anticipated that the effort behind nanowires research will proceed further to be implemented in daily electronic tools satisfying the demand of low-weight and small-size electronic devices.

**Keywords:** nanowires, semiconductors, silicon, CVD, catalyst, PV, AFM

## 1. Introduction

The topic of semiconductor nanowires is timely developing research. A legitimate question is then: what makes a material in a nanowire different from a bulk one? The direct answer is the extremely large surface-to-volume ratio. Any application occurs at the surface, such as chemical reactions; it will speed up at a medium of high surface area. Indeed, there are more features of integrating nanowires with the current available technologies (such as PV, AFM, and Raman spectroscopy) [1–5] and as stand-alone applications, such as sensors [6, 7]. Moreover, semiconductor nanowires can be functionalized and tailored in accordance with different requirements. For example, we can dope them with particular elements in the growth stage to change electrical properties or change the growth conditions to vary their shape or size.

There are several techniques of growing semiconductor nanowires. These fabrication methods are based on the semiconductor industrial capabilities, mainly top-down and bottom-up approaches. Photoresist patterning on top of a silicon-on-insulator layer followed by etching silicon and creating vertical silicon columns is explained as a top-down approach. Techniques based on the direct epitaxial growth of nanowires from a seeding material on a substrate are called bottom-up growth techniques, which is the main technique discussed in this chapter (see **Figure 1**).

Studies on silicon nanowires (Si-NWs) started with the pioneer work of Wagner and Ellis in 1965 [1]. The Vapor–Liquid–Solid (VLS) growth method uses metallic droplets or particles as a catalyst to nucleate the growth and absorb gaseous precursors and precipitate them into a solid form to permit crystal growth. The classic example is the VLS growth of Si-NWs on a Si substrate using gold (Au) eutectic droplets. Studying the structural properties of NWs is particularly important so that a reliable procedure of fabrication based on the desired functionality can be designed. Due to the enhanced surface-to-volume ratio in nanowires, their properties may depend critically on their surface condition and geometrical configuration. Even nanowires made of the same material may possess dissimilar properties due to differences in their crystal phase, crystalline size, surface conditions, and aspect ratios, which depend on the synthesis methods and conditions used in their fabrication. Moreover, the temperature of growing NWs is of critical importance, when we integrate them with other electronic devices so that the rest of the components of the electronic circuit do not get damaged at high temperatures. Si-NWs have been thus tried to be grown at low temperatures by utilizing metal catalysts, such as gold (Au) and Aluminum (Al), whose alloys with Si have low eutectic temperatures. Generally speaking, Si-NWs have been shown to provide a promising framework for applying the bottom-up approach (Feynman, 1959) for the design of nanostructures for nanoscience investigations and for potential nanotechnology applications. We are progressing in accordance with the predictions of Moore's Law, which suggests that the number of transistors in a dense integrated circuit doubles every two years [8]. Electronic devices are getting smaller and smaller, and the capabilities of these devices are becoming more leading-edge with the integration with the NWs technology.

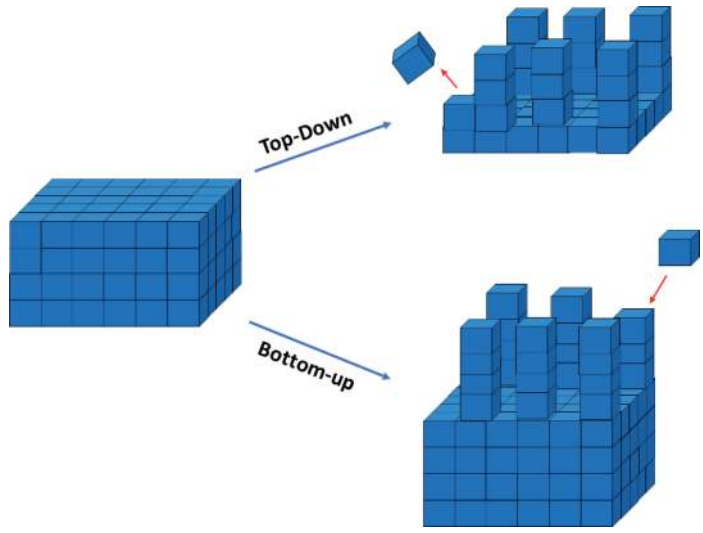



**Figure 1.**
*Schematic representation shows the original substrate, and the top main approaches of creating nanowires: Bottom-up and top-down approaches. Notice that the building blocks of materials (atoms) are moving toward (deposition) the substrate in the bottom-up process, while atoms are moving away (etching) from the substrate in the top-down mechanism.*

## 2. Semiconductor nanowires

The procedure of the bottom-up growth process of semiconductor NWs can be described as follows (see **Figure 2**); a semiconductor substrate, which could a bulk semiconductor substrate or an epitaxial layer of a semiconductor materials on a glass, for instance, (see **Figure 2**, step 1). A thin continuous layer of few nanometers-thick metal (step 2) evaporated on the surface of the semiconductor epitaxial layer, which segregates in isolated droplets during annealing (step 3). Precursor gas flows in the Chemical Vapor Deposition (CVD) reactor, where semiconductor atoms react at the metal-droplet surfaces, depositing semiconductor vapor atoms into solution within the metal droplets (step 4). The catalyst droplets supersaturate, inducing precipitation of crystalline semiconductor vapor atoms upon the substrate. As precipitation occurs only at the droplet metal (liquid)–semiconductor (solid) interfaces, the semiconductor atoms crystallite in wire structures with diameters comparable to the diameter of the metal droplet (step 5). This growth protocol has been called by Wagner and Ellis as VLS growth after the three coexisting phases: the vaporous precursors (such as $Si_v$), liquid catalyst droplets (such as $Au_l$), and solid silicon substrate ($Si_s$). Notice the possible incorporation of some of the metal atoms (Au) which

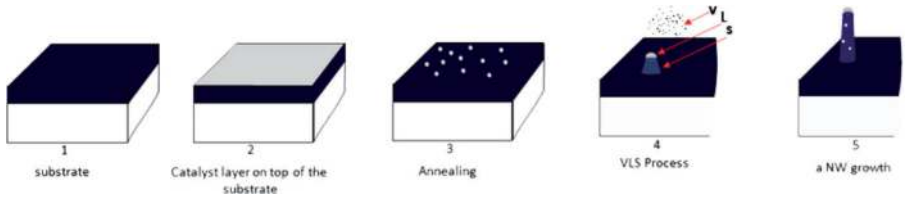



**Figure 2.**
*A schematic representation shows the sequence of the VLS process in five main steps. The substrate, depicted 1, can be bulk semiconductor materials or a relatively thin film of a semiconductor on a cheap substrate such as glass or polycarbonate (PC) or polymethyl methacrylate (PMMA) sheets; 2: Catalyst thin layer, 3: Catalyst after annealing where it balls up; 4: The sample was placed at the CVD reactor, allowing the precursor gas to flow; temperature reaches the eutectic; three phases coexist; and precipitation begins; and 5: Growth continues forming NWs.*

| Semiconductor materials | Growth techniques | Catalyst | References |
|---|---|---|---|
| $TiO_2/In_2O_3$ | Electron Beam Evaporation | Catalytic free glancing angle deposition technique | Guney et al. [9] |
| GaAs | Metal–organic chemical vapor deposition (MOCVD). A vapor–liquid–solid (VLS) mechanism | Au | Zeng et al. [10] |
| $SnO_2$ nanowires | A solvothermal process | Pd | Lu et al. [11] |
| p-type α-$Bi_2O_3$ | Vapor–Liquid–Solid (VLS) | different catalysts (Au, Pt and Cu) as seed layers but the highest aspect ratio was obtained using Au | Moumen et al. [7] |
| β-$Ga_2O_3$ | The chemical vapor deposition (CVD) method | Au catalysts | Miao et al. [12] |

| Semiconductor materials | Growth techniques | Catalyst | References |
|---|---|---|---|
| Si | CVD reactor | employing Sn nanospheres as catalyst | Mazzetta et al. [13] |
| InAs/InP | Molecular Beam Epitaxy (MBE) | gold catalyst | Helmi et al. [14] |
| Poly(3-hexylthiophene) (P3HT) nanowires | N/A | N/A | Jeong et al. [15] |
| Si-doped GaAs nanowires (NWs) | VS selective area growth patterned with SiO2 MBE | No catalysts | Ruhstorfer et al. [16] |
| II-VI semiconductors CdTe, CdS, ZnSe, and ZnS | Vapor–liquid–solid (VLS) process | Bismuth and tin | Yang et al. [17] |
| GaAs, InAs, and InGaAs nanowires | Molecular Beam Epitaxy (MBE) | Gold as the growth catalyst | Jabeen et al. [18] |
| Si | VLS-CVD | Al | Wacaser et al. [3] |
| Si NWs On Si(100) and Si(111) | VLS-CVD | Gold catalyst | Lindner et al. [19] |

**Table 1.**
*Published experimental research articles of semiconductor nanowires including the techniques and the catalysts.*

catalyzed the growth within the frame of the grown NW (Si-NW), as presented schematically in **Figure 2**.

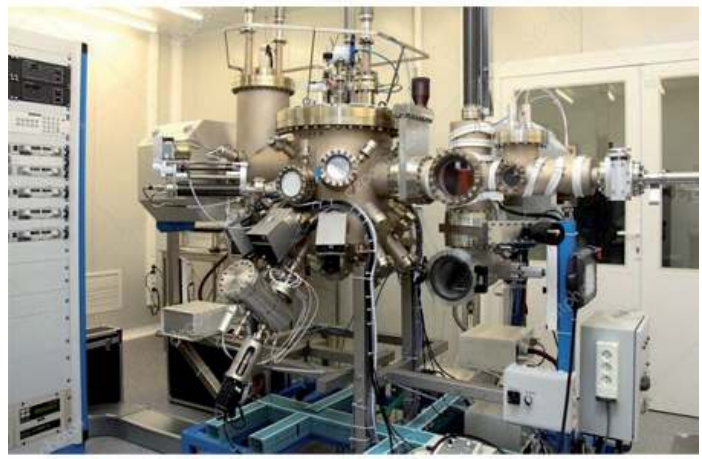
Semiconductor nanowires have been formed using various methods, as summarized in **Table 1**. Chemical Vapor Deposition (CVD) and Molecular Beam Epitaxy (MBE) have been the main growing systems since the past decade up to recent work for growing various semiconductor nanowires using several catalysts or without catalysts.

## 3. Epitaxial growth: Silicon nanowires

The nanowires growth is usually performed in a chemical vapor deposition (CVD) reactor or can be at the Molecular Beam Epitaxy (MBE); see **Figure 3**. The CVD growth mechanism involves the absorption of source material from the vapor phase into a liquid droplet of catalyst above the solid substrate as explained in the original work of Wagner and Ellis, in 1969 [20, 21]. The original proposed VLS mechanism of growing Si-NWs using Au as a catalyst is based on three critical parameters; the presence of the arriving Si **vapor** atoms to the metal droplet in a **liquid** state acting as a preferred position on the **solid** substrate. The detailed growth conditions at the CVD such as the pressure, flow rate, and temperature are placed accordingly. On the other hand, the motivation for using molecular beam epitaxy (MBE) to grow nanowires is that although MBE growth is both complicated and challenging, its high precision and flexibility can give good control over the growth of thin layers and abrupt junctions, which may be an advantage in future nanostructure devices [22].

According to the binary phase diagram of Si and Au, as shown in **Figure 4**, the lowest melting temperature for the Au–Si eutectic is approximately 363°C obtained for a composition of Si and Au. The eutectic is lower than the melting point of Au (1064°C) and Si (1414°C) [21]. Considering that the liquid phase is thermodynamically equilibrated with the solid one, the lowering of the melting point, with the size of the droplet, is given by Eq. (1), as follows [23]:

(a)



(b)

**Figure 3.**
*Photographs of (a) chemical vapor deposition (CVD) and (b) molecular beam epitaxy (MBE) systems (pictures were taken with permission from nanoscience Center, Cambridge, UK).*

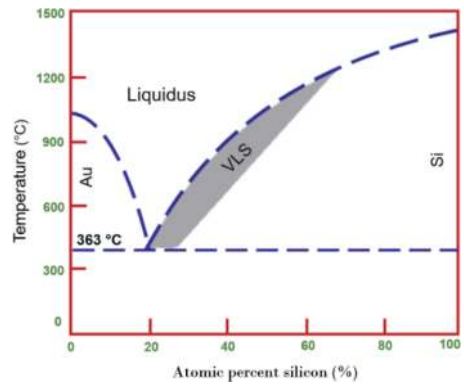



**Figure 4.**
*Phase diagram for the Au–Si system. The shaded zone represents the range of temperatures and alloy compositions at which VLS growth might occur [22].*

$$\delta T = 2\sigma.T_0 / (\rho.L.r) \quad (1)$$

where $\delta T$ is the lowering of the melting point, $\sigma$ is the interfacial energy, $T_0$ is the melting point of the bulk metal, $\rho$ is the density of the material,

$L$ is the latent heat, and $r$ is the radius of the circle of the catalysts. Thus, heating Au film deposited on a Si substrate to a temperature of 363°C results in the formation of liquid Au–Si eutectic. The eutectic is simply a mixture of two elements at such proportions that its melting point is at the lowest possible temperature, much lower than the melting point of either of the two elements that make it up. If these Au–Si melted alloys are placed in an environment containing a gaseous silicon precursor such as silane ($SiH_4$), the precursor molecules decompose into Si and $H_2$ at the outer surface of the metal droplets, thereby supplying additional Si to the Au–Si alloy, and precipitate at the interface between the liquid alloy droplet and the solid substrate.

It has been shown that Si-NWs grow perpendicularly on Si(111), as represented in **Figure 5**.

A variety of derivatives of CVD methods exist, which can be classified by parameters such as the base and operation pressure or the treatment of the precursor. Since Si is known to oxidize easily, it is a key parameter for a successful epitaxial growth of Si-NWs to reduce the oxygen background pressure. In particular, when oxygen-sensitive catalyst materials are used, it turns out to be useful to combine catalyst deposition and nanowire growth in one system, so that growth experiments can be performed without breaking the vacuum in between [24, 25].

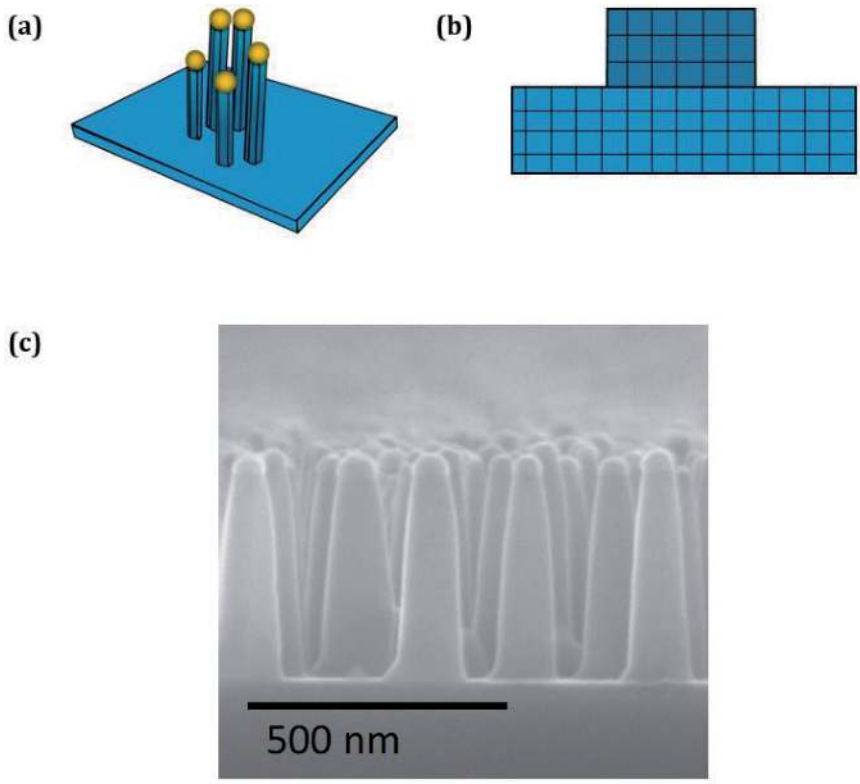



**Figure 5.**
*Schematic representation of epitaxial growth of Si-NWs (a), where the grown nanowires copy the crystal structure of the substrate, (c) epitaxial grown Si-NWs on Si(111) substrate catalyzed with Al. Detailed growth conditions can be found in Khayyat et al. [24].*

It is often noted in VLS wire growth that the radius of the catalyst droplet exceeds the radius of the nanowire Eq. (2) [22].

$$R = r\sqrt{1/\left(1-\left(\sigma_{ls}/\sigma_{l}\right)^{2}\right)} \tag{2}$$

where $R$ is radius of the catalyst droplet, $r$ is the radius of the nanowire, $\sigma_l$ is the surface tension of the liquid catalyst, and $\sigma_{ls}$ is the surface tension of the liquid–catalyst interface. Based on this, one can estimate the growth conditions and deduce the diameters of the catalyst droplet of the resulted growth of NWs with a certain average diameter.

## 4. Si-NWs as building blocks for bottom-up nanotechnology

Controlling the growth position of an NW is important for fabricating devices, especially when involving a large array of nanowires. The growth reproducibility is critically a key parameter in the progress of implementing nanowires in advance applications.

Free-standing nanowires can be yielded and their position on the wafer can be determined by predefining the position of the seed on the wafer using lithography. There are several research groups working on optimizing the growth of positional Si-NWs [1, 26–28]. Most of the studies till date have used Au due to the convenience of handling that arises from its resistance to oxidation. The current technique is a new method of controlling the position of the grown Si-NWs seeded with oxygen-reactive materials such as Al, which is a standard metal in silicon industrial process line. The technique is based on electron beam lithography for patterning the Si substrate and then forming a Si alloy with Al during a subsequent annealing step. Moreover, it does not require removal of the patterned compound oxide layer [25].

### 4.1 Nanoscale chemical templating (NCT) technique

It is an innovative technique that arises as a solution of the issue of the defective planar growth between the grown Si-NWs seeded with Al (or any other chemically active elements). The technique is called Nanoscale Chemical Templating (NCT) of oxygen-reactive elements. Now, what makes NCT an innovative solution? [25].

I. Does not require Al removal for selective growth.

II. Does not require any lithography steps.

III. Multiple application space.

As explained in **Figure 6** (I), the process that does not require Al removal (I-a) shows the patterned $SiO_2$ layer after photolithography, etching, and resist removal. (I-b) After Al deposition and annealing, notice the agglomerated Al:Si feature where it balls up in the openings forming the NW seeds, while the Al in contact with $SiO_2$ has reacted forming $Al_2O_3$. (I-c) After NW growth. The NWs are epitaxial and appear as bright spots in the plan view. In the cross sectional view, tapering is visible, due to a thin, non-seeded, Si layer approximately thinner than 1/100 of the length of the nanowire. Notice that a single NW per opening is achieved. (I-c3) and

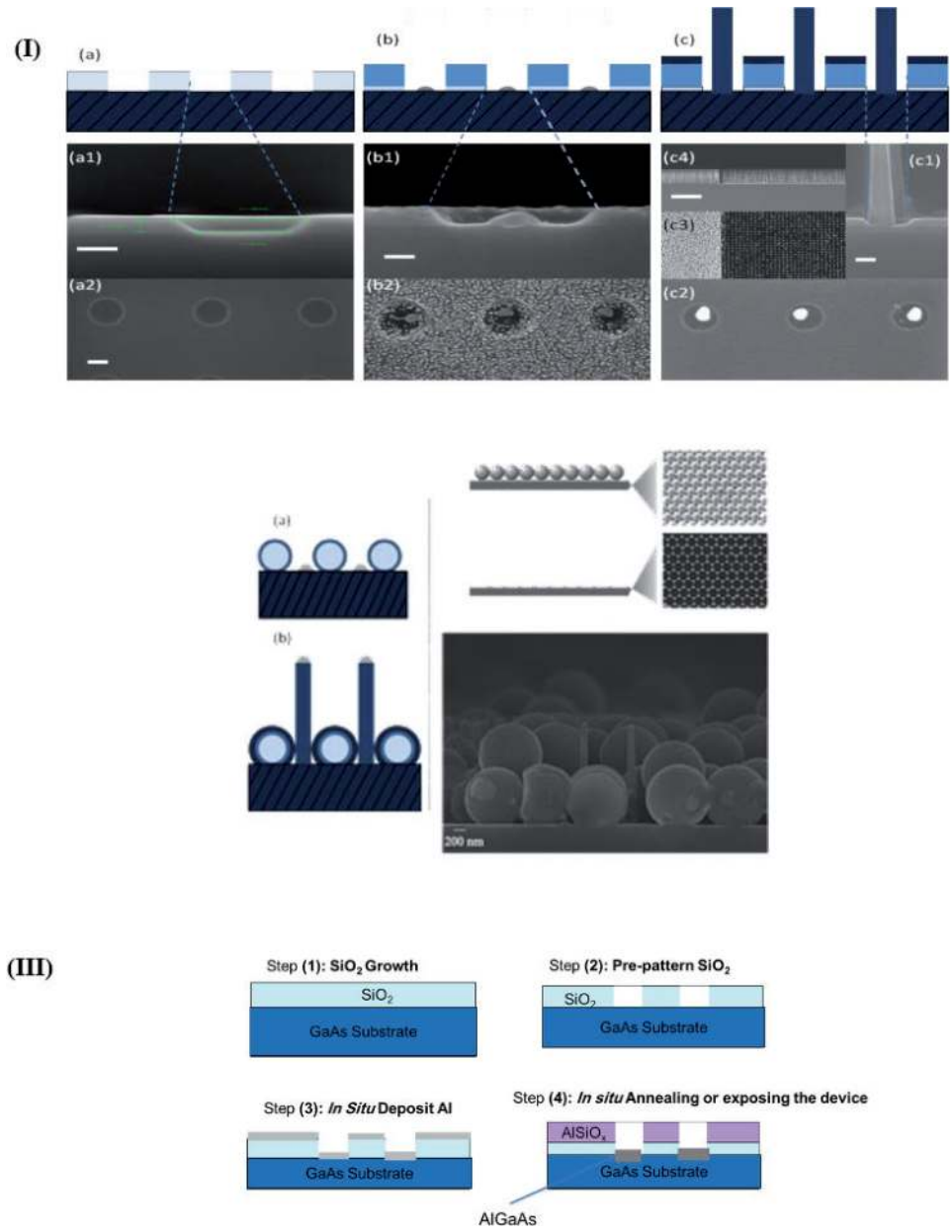



**Figure 6.**
*(I) (a)–(c) schematic illustration of NCT of NWs with corresponding SEM images, cross sectional ((a1), (b1), (c1) and (c3)) and plan views ((a2), (b2), (c2) and (c4)). The scale bars are: (a1) and (b1) 100 nm; (c1) 300 nm; (a2), (b2), and (c2) 1 μm; and (c3) and (c4) 20 μm. (II) representation of NCT using silica microspheres (a& b) and the corresponding SEM original proof of the concept. (III) schematic representation of the selective growth of AlGaAs for further applications.*

(I-c4) show a larger area containing both a patterned area on the right and an area with no oxide on the left where random growth occurs.

The position control of Si-NWs can be achieved using silica microsphere, as described in 6 (II). The schematic representation of a spinning silica microsphere on the Si substrate, followed by thin-layer evaporation of Al and the subsequent annealing, is shown in (a), where (b) shows the Si-NWs growth. Moreover, patterning III-V semiconductors selectively is considered as one of the possible multiple applications schemes (III).

### 4.2 Applications on NCT: functional devices of Si-NWs

It is of great interest to find applications for Si-NWs, which could be as stand-alone innovative structures such as in photovoltaic (PV) cells (**Figure 7**) or integrating with conventional structures such as Atomic Force Microscopy (AFM) (**Figure 8**) [26], and MOSFET (**Figure 9**), for the purpose of developing and miniaturizing.

**PV Cells** made of Si-NWs have several potential benefits over conventional bulk Si one- or thin-film devices related primarily to cost reduction. It is possible to form the p–n core–shell junctions in high-density arrays, which have the advantages of decoupling the absorption of light from charge transport by allowing lateral diffusion of minority carriers to the p–n junction which is at most 50–500 nm away rather than many microns away as in Si conventional bulk photovoltaic cells. Based on this, the potential cost benefits come from lowering the purity standard and the amount of semiconductor material needed to obtain sophisticated efficiencies, increasing the defect tolerance, and lattice-matched substrates [6]. The concept of

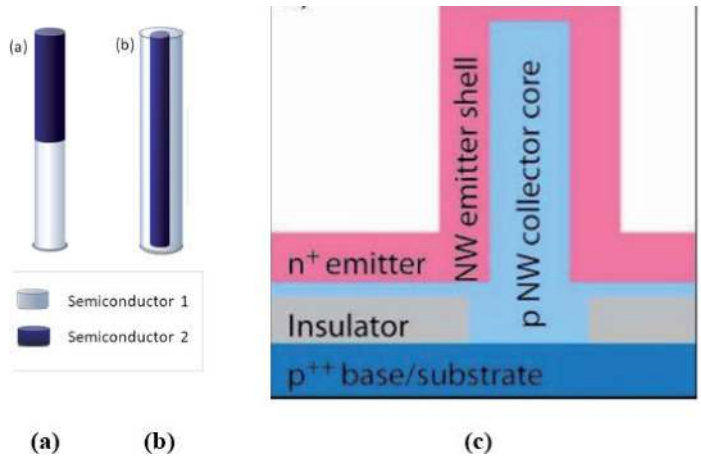



**Figure 7.**
*Schematic illustration of the main types of heterojunction nanowires. (a) Axial heterojunction. (b) Radial heterojunction (core-shell). (c) a core–shell PV cell [3].*

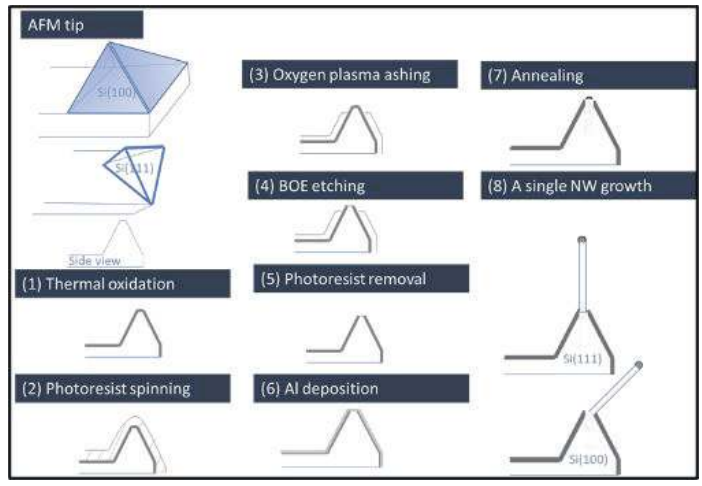



**Figure 8.**
*Schematic demonstration of detailed steps involved in Si-NWs integration with AFM tip [26].*

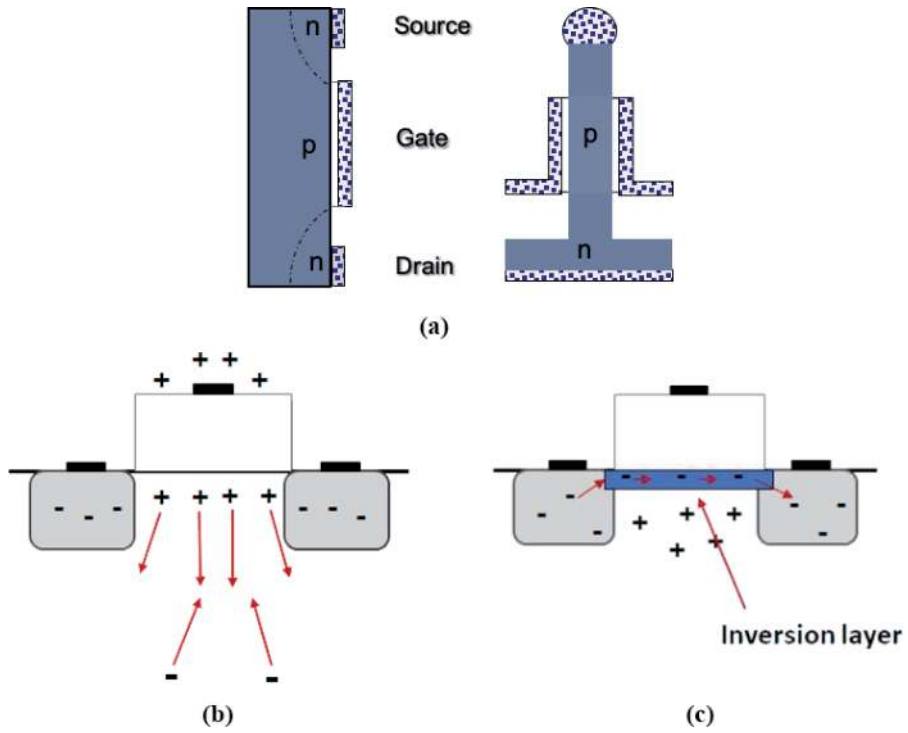



**Figure 9.**
*(a) Shows a schematic representation of an (npn) MOSFET, the conventional one in parallel with the innovative one of NWs; (b) shows the migration of charges based on the applied voltages; and (c) presents the formation of the inversion layer, the channel across the diameter of the NW.*

nanowire-based solar cells has attracted significant attention because of their potential benefits in carrier transport, charge separation, and light absorption. The Lieber [1] and Atwater [28] and other groups [29–31] have developed core–shell growth and contact strategy for their silicon p–i–n nanowire solar cells, with sophisticated efficiencies. Moreover, the ability to make single-crystalline nanowires on low-cost substrates, such as Al foil, and to relax strain in subsequent epitaxial layers removes two more major cost hurdles associated with high-efficiency planar solar cells. A schematic representation is shown in **Figure 7** where $SiO_2$ has been used as a separation layer between the planar defective growth, which occurs during NWs growth, and the substrate to enhance the performance of the PV core–shell junctions [3].

**AFM** was invented in 1968, which has opened new perspectives for various micro- and nanoscale surface imaging in science and industry. Nanotechnology has benefited from the invention of the AFM, and in turn AFM is developing based on the progress of Si-NWs growth techniques. Based on the NCT technique that is based on catalyzing the growth of Si-NWs with Al, it has been proposed to improve the resolution of AFM tips in a production scale [26]. The concept of "Production Scale Fabrication Method for High Resolution AFM Tips" is demonstrated in **Figure 8**, along with the various steps of the Si-NW growth on the tip of the available Si(100) or Si(111) AFM tips. The grown Si-NW on the squared-base Si(100) tip is 45° tilted, while Si-NW grow perpendicularly on the AFM tip of the triangular base of Si(111) [32–35] where further reduction of the average wire diameter to the nanometer scale can be done via hydrogen annealing or oxidation [8, 36–41]. As the diameter decreased, the tensile strength tended to increase from 4.4 to 11.3 GPa. Under bending, the Si-NWs demonstrated considerable plasticity [42].

The proposed structure in **Figure 8** has not yet been experimentally demonstrated [26]; the fabrication of the structure could be achieved by the described processes where it illustrates the potential mass scalability of this technique. A strategy has been

presented to equip microcantilever beams with single Si-NW scanning tips that were directly grown by Au-catalyzed VLS synthesis. It was evident from AFM measurements evidently that the assembled Si-NW scanning tips are suitable for topography reconstruction as well as for overall comparison with conventional pyramidal scanning tips besides their high aspect-ratio nature and a superior durability [39, 43–45].

**MOSFET** can be designed in the form of NWs, as shown in **Figure 9** [8]. The channel can be altered using NWs as shown when a positive voltage is applied to the gate. The holes in the p-type Si are repelled from the surface, and minority carrier conduction electrons are attracted to the surface. If the gate voltage exceeds the threshold value, then an inversion layer is created near the surface. In this layer, the material behaves as an n-type and provides a conducting channel between the source and the drain. The width of the conduction channel is dominated by the diameter of the NW.

Because of the enhanced surface-to-volume ratio of NWs, their transport behavior may be modified by changing their surface conditions, and this property may be utilized for sensor applications to provide improved sensitivity compared to conventional sensors based on bulk material. Si-NWs sensors will potentially be smaller, more sensitive, demand less power, and react faster than their macroscopic counterparts [42, 43, 46].

## 5. Future remarks of nanowires research

In this chapter, we attempt to summarize progresses made in this field during the last several years, ranging from nanowire growth with precise control at the atomic level [41]. Probing novel properties in 1D systems using a stand-alone innovative novel device was presented, in addition to integration and assembly methods of large numbers of NWs for practical applications.

We conclude this chapter with some outlooks for future research. Will nanowires research lead to new science or discovery of new phenomena? Will it lead to new applications? [47–50]. The answer is clearly yes based on the research activity done on the topic of nanowires. Studies are among the most potential in the topic of nanoscience, as shown in **Figure 10**. The cumulative published studies starting from 2010 up to 2020 on the topic of nanowires have been increased, thus markedly reflecting the technological importance of this topic.

The ever-growing demand for smaller electronic devices is prompting the scientific community to produce circuits whose components satisfy the size and weight requirements. The well-controlled NW growth process, with distinct chemical composition, structure, size, and morphology, implies that semiconductor nanowires can be integrated within the process of the development of nanodevices. Control of the synthesis and the surface properties of Si-NWs may open new opportunities in the field of silicon nanoelectronics and use them as nanocomponents to build nanocircuits and nanobiosensors. Moreover, Si-NWs possess the combined attributes of cost effectiveness and mature manufacturing infrastructures [51–55].

The conventional thin-film technologies grown at MBE have technical limitations, mainly the interfacial lattice mismatch issues that often result in highly defective optical materials. In this regard, Si-NWs growth provides a natural mechanism for relaxing the lattice strain at the interface and enables dislocation-free semiconductor growth on lattice-mismatched substrates, where radial strain relaxation allows for uncharted combinations of semiconductor materials (III–V on Si). In this regard, efforts must be made to break new grounds in this promising research field to stimulate more creative ideas about nanowire research and applications. Many

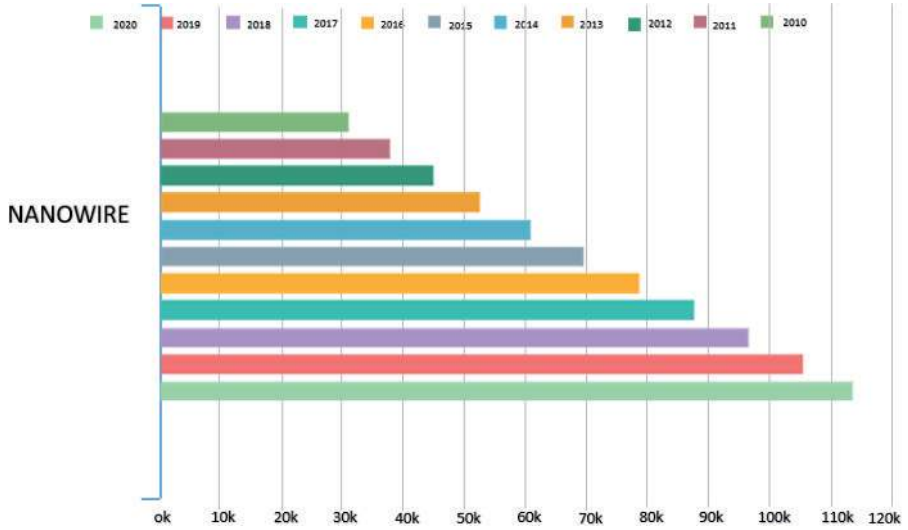



**Figure 10.**
*Cumulative nanowires publications in 11 years 2010–2020 (there are no data available for 2021, where the x-axis represents the number of articles in kilo. In 2020, there were more than 100,000 articles on the topic on nanowires, according to the number of nanotechnology-related articles indexed in web of science (WoS) (ISI web of knowledge). https://statnano.com/report/s29/3.*

promising applications are now at the early demonstration stage but are moving ahead rapidly because of their promise for new functionality, not previously available, to the fields of electronics, optoelectronics, biotechnology, magnetics, and energy conversion and generation, among others [56, 57].

Integration of nanoelectronic units, such as Si-NWs, and biosystems is a multidisciplinary field that has the potential for multilateral impact on various scientific fields including biotechnology. The combination of these multidisciplinary research backgrounds promises to yield revolutionary advances in our everyday life through, for example, the creation of new and powerful tools that enable direct, sensitive, and rapid analysis of biological and chemical species [49, 50].

To simulate future research on NWs, one would look at the progress achieved by the industries of semiconductors which have produced devices and systems that are part of our daily lives, including transistors, sensors, lasers, light-emitting diodes, solar panels, computers, and cell phones [51–54, 58]. Then, imagine changing the morphology of semiconductors from the bulk to the nanowire form; one might wonder how much fundamental difference there is. Where, sometimes the intersection of top-down and bottom-up approaches toward building nanostructures for practical functionality is also possible.

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## Conflict of interest

The author declares no conflict of interest.

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